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Opto-Electronics Review 26 (2018) 63–72

Contents lists available at ScienceDirect

Opto-Electronics Review

journal homepage: http://www.journals.elsevier.com/opto-electronics review

Realization of XNOR logic function with all-optical high contrast XOR and NOT gates

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ARTICLE INFO

Article history:
Received 24 April 2017
Received in revised form 1 December 2017
Accepted 22 January 2018
Available online 8 February 2018

Keywords:
High contrast outputs
T-shaped waveguide
Realization
Cascade

ABSTRACT

In this article, we propose the realization of XNOR logic function by using all-optical XOR and NOT logic gates. Initially, both XOR and NOT gates are designed, simulated and optimized for high contrast outputs. T-shaped waveguides are created on the photonic crystal platform to realize these logic gates. An extra input is used to perform the inversion operation in the NOT gate. Inputs in both the gates are applied with out of phase so as to have a destructive interference between them and produce negligible intensity for logic '0'. The XOR and NOT gates are simulated using Finite Difference Time Domain method which results with a high contrast ratio of 55.23 dB and 54.83 dB, respectively at a response time of 0.136 ps and 0.1256 ps. Later, both the gates are cascaded by superimposing the output branch of the waveguide of XOR gate with the input branch of the waveguide of NOT gate so that it can be resulted with compact size for XNOR logic function. The resultant structure of XNOR logic came out with the contrast ratio of 12.27 dB at a response time of 0.1588 ps. Finally, it can be concluded that the proposed structures with fair output performance can suitably be applied in the design of photonic integrated circuits for high speed computing and telecommunication systems.

1. Introduction

Increase in the demand of high speed computing and telecommunication systems escalates the need of all-optical devices. All-optical devices increase the speed of processing in Tera bits per second (Tbps) and provide compactness due to lack of Optical - Electrical-Optical (O-E-O) conversion [1,2]. Another fact that comes into picture related to the increase in speed is the data processing in those devices, and this happens nearly with the speed of light, but medium should be considered as it also matters the speed. In recent years, to increase the data processing speed, researchers have been concentrating more on the design of all-optical logic devices which are part and parcel of telecommunication networks and computing systems. Many methods have been followed for such, among them the Semiconductor Optical Amplifiers [3–6], nonlinearity [7], Fiber Bragg Gratings (FBGs) [8], etc. But each one has its own limitation such as spontaneous emission of noise [9], high power consumption [10] and large size [8], etc. In order to overcome these limitations, scientists are working towards the invention of artificial optical materials which can reduce the size, give fast response and low power consumption, etc. Among them, photonic crystal is one of the most promising material the researchers are concentrating for the design of all-optical logic devices.

Photonic Crystal (PhC) is an artificial optical material with a periodic variation of dielectric constant in one dimension or two dimensions or all the three dimensions, and it exhibits Photonic Band Gaps (PBG) [11]. Photonic band gap is a range of wavelengths of light which are disallowed by the photonic crystal to pass through it. Band gap engineering alongside the introduction of defects into the PhCs assists in the modelling of logic designs [12]. Basically, a Two Dimensional (2D) PhC is used for the sake of these designs wherein an array of dielectric rods are arranged in two directions with air host. Changing the parameters of a particular rod(s) such as dielectric constant, shape, spacing between the rods and lattice type is called as defect(s).

In the design of the PhC based all-optical logic designs such as logic gates, adders, demultiplexers, flipflops etc, several phenomena have been used, among them interference [2,13–24], resonance [1,25–27], self-collimation [28–30] are the few. Linear and/or nonlinear optical materials are being used except in self-collimation which depends only on linearity [30]. High contrast outputs are possible with interference [31] but at the cost of structural complexity and large size. Moreover, the designs which depend upon multimode interference and need phase of the input light for data

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https://doi.org/10.1016/j.opelre.2018.01.003
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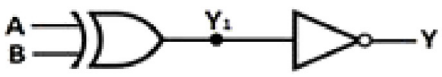
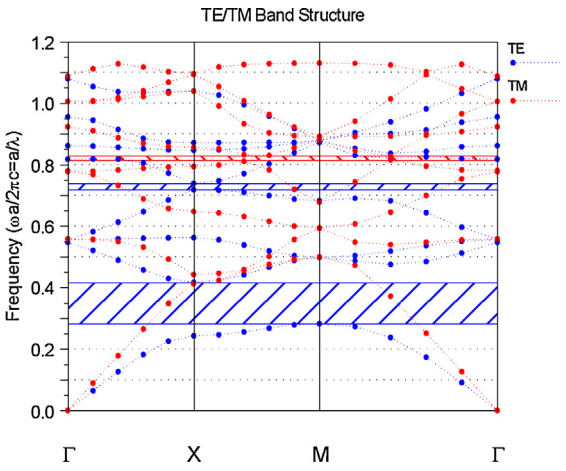


A	B	$Y_1 = A \oplus B$	$Y = A \odot B$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

(a)



(b)

Fig. 1. a) Realization of XNOR logic function using XOR and NOT gates (above) and its truth table (below), and b) band diagram of uniform 2D PhC lattice.

processing too provide high contrast outputs [14,15]. All-optical logic gates with high contrast output helps in cascading with each other to realize a particular logical or Boolean function. In the proposed work, high contrast logic gates *viz.*, XOR and NOT are designed using simple PhC based T-shaped waveguide with less complexity. Further, they have been cascaded to realize the XNOR logic function. These equivalence gates viz., XOR and XNOR are very much useful in error correcting techniques in data communication. These logic gates with all-optical nature increase the speed of computation required for error correction, in turn suite themselves in high speed telecommunication and computing applications. The proposed XOR and NOT gates are resulted with output contrast ratio of above 50 dB, and XNOR with more than 12 dB at fast response time.

The latter part of this article is structured as follows. Section 2 discusses on the design and simulation of high contrast output XOR and NOT gates. Section 3 describes the realization of XNOR logic function using XOR and NOT gates followed by Section 4 which discusses on the comparison of the designed gates with the existing one. Finally, Section 5 concludes the proposed work.

2. High contrast all-optical XOR and NOT logic gates

The logic function of XNOR is the complement of XOR, it means, the output from the XOR gate is to be complimented using NOT gate as shown in Fig. 1(a). The logic function of Y_1 and Y are given below

$$Y_1 = \overline{A}B + A\overline{B} = A \oplus B \tag{1}$$

$$Y = \overline{Y_1} = \overline{\overline{A}B + A\overline{B}} = \overline{A \oplus B} = AB + \overline{A}\overline{B} = A \odot B. \tag{2}$$

Cascading of XOR and NOT gates provides the XNOR logic function. In order to cascade all-optical logic gates, they should have high output contrast ratio which prevents the output power levels to degrade so as to have a higher distinction between the binary logic levels (i.e., logic '0' and logic '1'). Thus, in the proposed work, initially XOR and NOT logic gates are designed and simulated for high contrast outputs, and then they are cascaded to achieve XNOR logic function. Initially, Plane Wave Expansion (PWE) method is used to calculate the PBG's of uniform 2D PhC on which the logic gates are to be created. From that it has been observed that there are three PBGs as illustrated by the band diagram shown in Fig. 1(b). Among the three, two bands are of TE mode and one is of TM mode, and from these three bands only one TE band is chosen which accommodates into communication window. This TE band offers a wavelength range of 1440 nm–2120 nm (0.282568 (a/λ) to 0.416924(a/λ)) which is being reflected by the PhC considered for the design.

To design these two gates, a simple T-shaped waveguide is used with optimized radii of the additional rods. In these logic gates, the intensity of the light defines the binary logic levels. At the input, no light is considered as logic '0' and a light intensity is considered as logic '1', whereas at the output, a light intensity which is as low as 2.5% (output transmission of 0.025) of the applied input is considered as logic '0' and an intensity of above or equal to 40% (output transmission of 0.4) of the applied input is considered as logic '1'. These values are chosen such that the output contrast ratio should be above 10 dB, and the output contrast ratio (CR) is given as

$$CR = 10 \log \frac{P_1}{P_0}, \tag{3}$$

where P_0 and P_1 are the output power levels achieved for logic '0' and logic '1', respectively. This parameter discriminates the logic levels at the output, and a far lower value of P_0 for logic '0' provides a very high contrast ratio.

2.1. Design and simulation of XOR gate

A T-shaped waveguide is created in 2D PhC, comprises of an array of 21 × 15 *Si* rods in air host with square-type lattice as shown in Fig. 2(a). It consists of two input ports *A* and *B*, and an output port Y_1 with some additional light bending rods R_{s1}, R_{s2}, and R_a at the junction. The radius of each *Si* rod (except additional rods) in the PhC is 0.2*a*, where *a* is the lattice constant of value 600 nm. The additional rods R_{s1}, R_{s2}, and R_a are optimized to 72 nm, 30 nm and 48 nm, respectively in such a way that an acceptable output transmission with lower reflection can be achieved, where transmission is the ratio of output power P_{out} and the applied input power P_a.

The lengths of input branches of the waveguide of XOR gate are same, and so the light signals from both the input ports interfere constructively or destructively at a phase difference of 0° or 180°, respectively. In order to achieve a negligible intensity at the output Y_1 for the last case of the truth table shown in Fig. 1(a), the input ports *A* and *B*, excited with light signals are to be destructively interfered. Thus, in the proposed structure, the input light signals at ports *A* and *B* are applied with phase 0° and 180°, respectively so

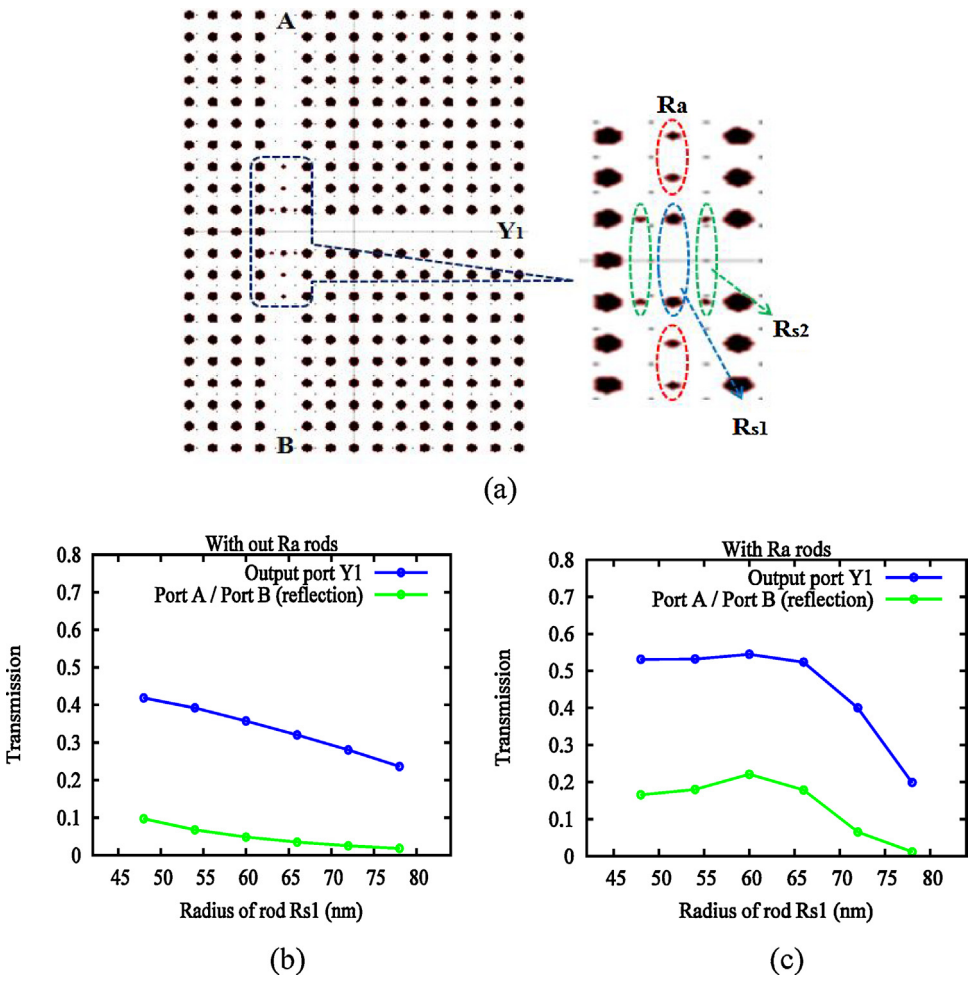


Fig. 2. Proposed XOR gate a) lattice structure, b) effect of rods R_{s1} on the output transmission without rod R_a, and c) effect of rods R_{s1} on the output transmission with rod R_a.

as to have a destructive interference between them and produce a very low intensity at port Y_1. This is the basic requirement of the proposed structure to work as XOR gate. When either of the input ports (A or B) is excited, the light signal from the concerned input port will get diverted to the output port Y_1 due to the light bending rods R_{s1} and R_{s2}, and it can be read as logic '1'. In these two cases, phase of the input light (either 0° or 180°) doesn't affect the light intensity at the output Y_1 as there is no interference at the junction due to lack of the other input. The 180° phase of the input light is assumed to be obtained externally as it allows perfect destructive interference. The phase shifter can also be proposed internally in the waveguide branch of port B using MMI based cavity as same as in the reported half adder [17]. But the MMI based cavity which is being used as phase shifter may not provide the phase as exact as it is provided by the external phase shifter.

The reflector rods R_a besides the rod R_{s1} improves the transmission which can be observed from Fig. 2(b) and 2(c). As the figures show, with R_a rods, the output transmission for single input port excitation is higher than the structure without these rods. As the radius of the rod R_{s1} increases, the output transmission decreases but with reduced reflection into the unemployed input port. The analysis on the additional rods has been done by taking the radius of R_a as two third of the radius of R_{s1}. From Fig. 2(c), it can be said that the acceptable output transmission with low reflection is possible at R_{s1} = 72 nm and R_a = 48 nm, where the output transmission is above 0.4 which can be read as logic '1' as per the threshold power levels that were assumed previously. Without these R_a rods, as shown in Fig. 2(b), the output transmission is less than 0.3 with low reflection at R_{s1} = 72 nm which cannot be read as logic '1'. Thus, the rods R_{s1} and R_a are optimized to 72 nm and 48 nm, respectively, and the rod R_{s2} is kept at one fourth of the radius of the normal rod.

Simulation is carried out by applying input light of 1550 nm using Finite Difference Time Domain (FDTD) method on the proposed XOR gate with the optimized rods R_{s1} = 72 nm, R_{s2} = 30 nm and R_a = 48 nm. Perfectly matched boundary conditions are employed in order to absorb the waves and avoid the reflections at the boundary. The electromagnetic waves propagate in the (x, z) plane with magnetic field polarization to be in parallel with the axis of the *Si* rods, i.e., y-axis. In order to guarantee the convergence in the simulation, space grids are chosen such that $\Delta x < \lambda/10$ and $\Delta z < \lambda/10$, where x and z axes are the horizontal and vertical direction coordinates, respectively. Stable simulations can be achieved by choosing the space grid and the time grid in such a way that the following Courant condition [13] can be satisfied

$$c\Delta t < \frac{1}{\sqrt{(\Delta x)^{-2} + (\Delta z)^{-2}}}. \quad (4)$$

The electric field distribution of the proposed XOR gate is shown in Fig. 3 when the input signals are applied in accordance with the truth table. When one of the input ports (either A or B) is excited with light signal, an output transmission of 0.4 is achieved at port Y_1 which can be read as logic '1', and this is due to the additional rods at the junction. When both the input ports are excited with out of phase light signals, a destructive interference occurs at the junction and a very negligible amount of output transmission (light intensity) of value 0.0000012 is observed at port Y_1, and this can be read

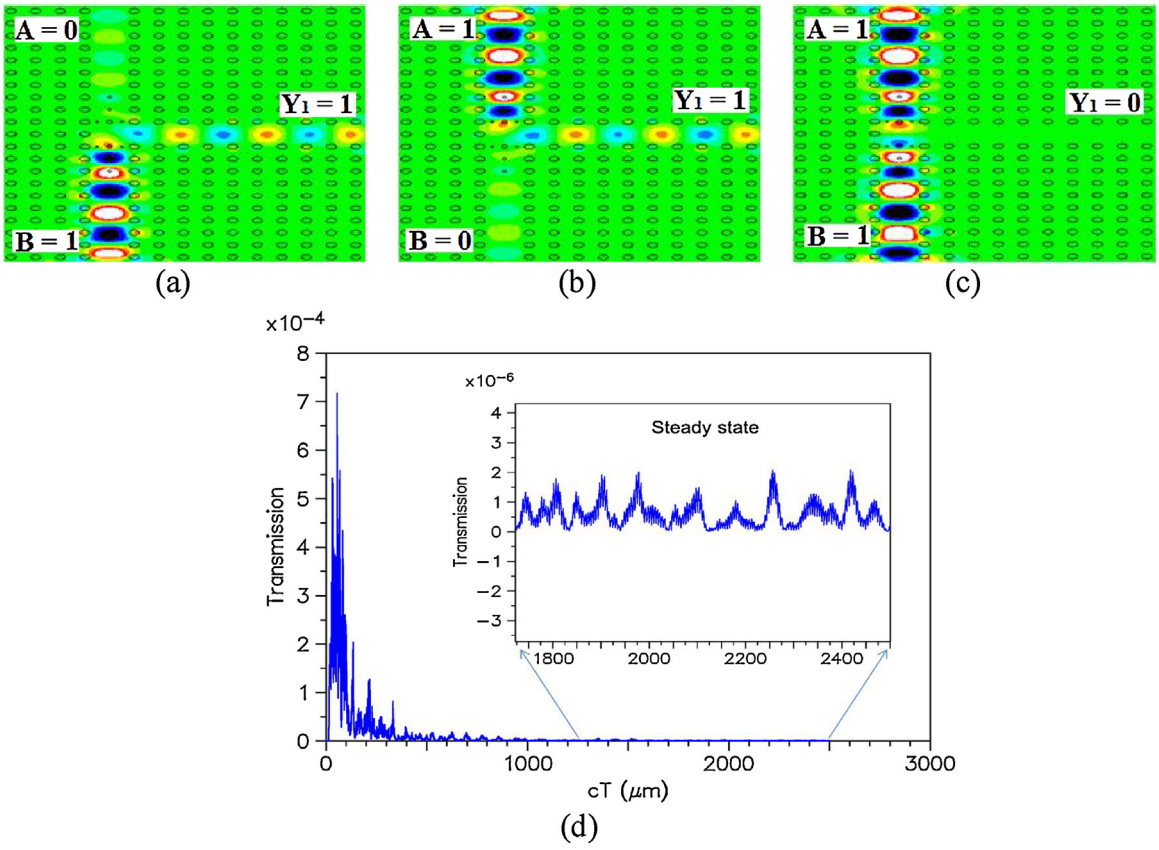


Fig. 3. Electric field distribution of the proposed XOR gate for inputs a) A = 0, B = 1, b) A = 1, B = 0, c) A = B = 1, and (d) transmission for logic '0 in steady state.

as logic '0'. This negligible transmission of logic '0' can be observed from Fig. 3(d) wherein the steady state response is shown, and it is being considered as the power level of logic '0'. This negligible value of the output intensity is achieved due to the perfect destructive interference occurs between the inputs. The basic reason behind this is the symmetric input excitation, i.e., the two branches of the T-shaped waveguide (*A* and *B*) which are equal in length and structural variations are being used as input ports, and are being excited to get the output. The output contrast ratio is calculated from Eq. (3), and it is 55.23 dB which is higher than the XOR gates existing in the literature so far. This has become possible due to the smaller output power achieved for logic '0' as this lower value increases the contrast ratio highly.

The response time of the proposed XOR gate is calculated from the time evolving curve [2,13] shown in Fig. 4. From the figure, it can be observed that the time (T) required for the proposed structure to produce the output from 0 to 90% of the average output power P_{avg} is 0.0944 ps (cT = 28.3 μm), where c is the speed of the light in vacuum. This time T comprises two components, one is transmission delay (t_{11}) which is the time required by the structure to move from 0 to 0.1% of the P_{avg}, and another one is the time (t_{12}) required to move from 0.1 to 90% of P_{avg}. These time components can be calculated using the respective values on the x-axis and the value of c. From the time evolving curve, the values of these two components are determined, and they are t_{11} = 0.0604 ps (18.13 μm) and t_{12} = 0.034 ps (10.18 μm). As the structure is only dependent on linear materials, the falling time from P_{avg} to 10% of P_{avg} can be expected to be same as that of t_{12} [2,13]. So, the width of a narrow pulse is of $2 \times t_{12}$ = 0.068 ps. Hence, a response time of 0.136 ps is achieved for a complete period of 50% duty cycle. All the observations on the output performance of the proposed XOR gate are summarized and represented in Table 1.

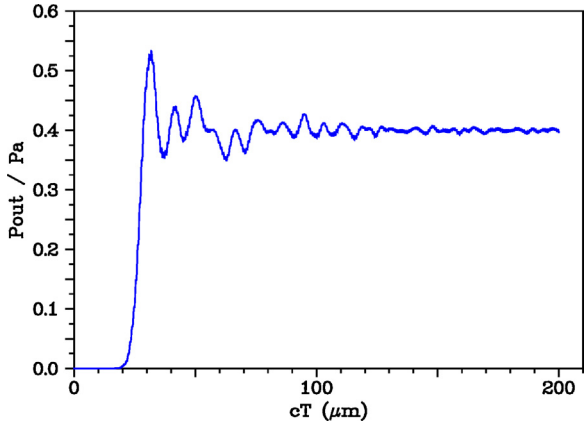


Fig. 4. Time evolving curve from the proposed XOR gate.

Table 1
Output performance of the proposed XOR gate.

Input		Output (Y_1)			
A	B	Transmission (P_{out}/P_a)	Logic	Contrast ratio	Response time
0	0	0	0	55.23 dB	0.136 ps
1	0	0.4	1		
0	1	0.4	1		
1	1	0.0000012	0		

2.2. Design and simulation of NOT gate

Basically, a NOT gate consists of one input and one output, which can invert or compliment the input. The internal schematic of

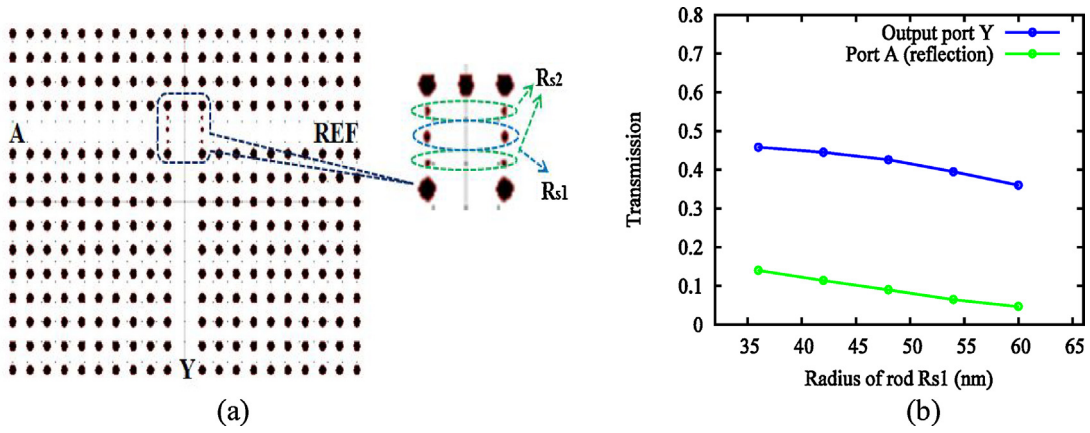


Fig. 5. Proposed NOT gate a) Lattice structure, and b) Effect of R_{s1} rod on the output transmission.

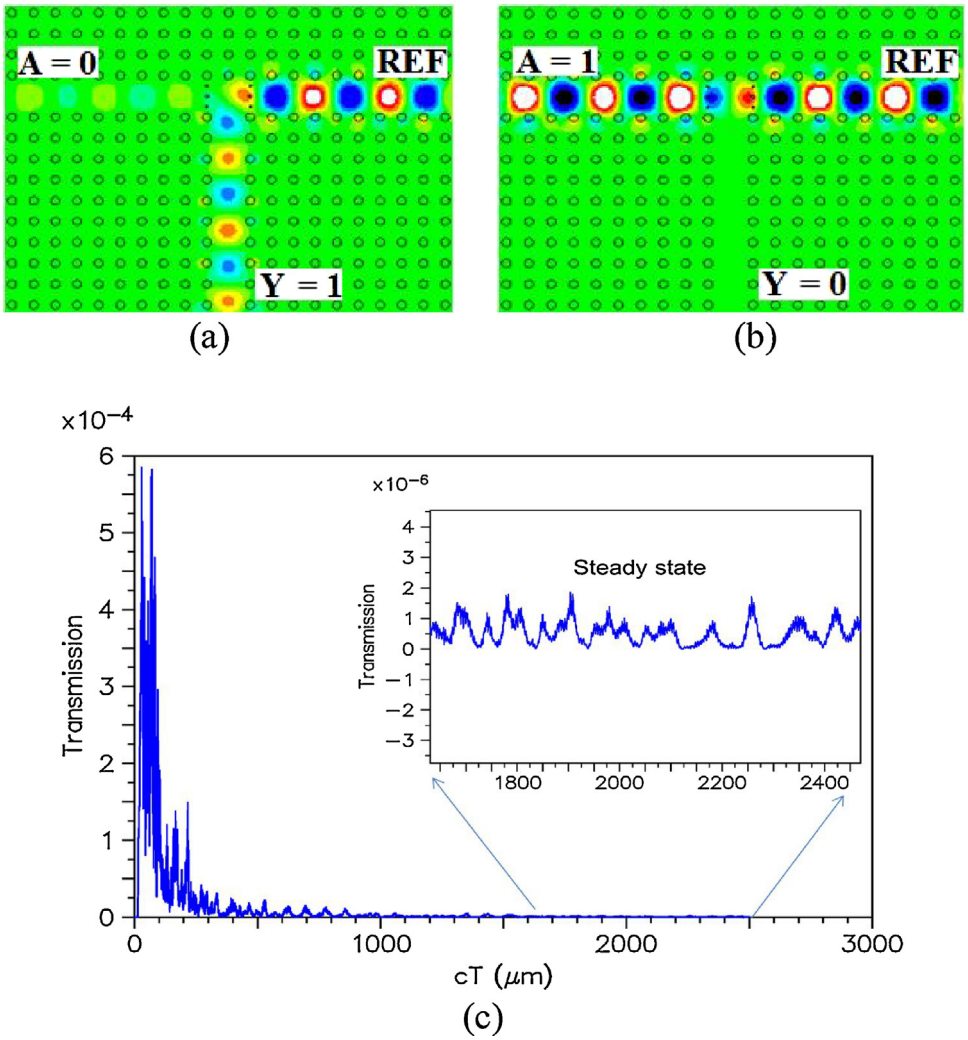


Fig. 6. Electric field distribution of the proposed NOT gate for a) A = 0, b) A = 1, and c) transmission for logic '0 in steady state.

the logic gates available in digital Integrated Circuits (IC) consists of power supply inputs which are responsible to produce output logic '1' when input is logic '0'. Similarly, in optical based logic designs there need an input power supply to produce output logic '1' (light intensity) when inputs are not applied. For example in optical based logic gates like NOT, NOR, NAND, and XNOR, and also in designs wherein output logic '1' to be produced without applying the inputs. In the proposed NOT gate, an extra input called as reference input (REF) is used in order to produce the output logic '1' when input is zero.

The same T-shaped waveguide is used as a NOT gate but without the reflector rods as shown in Fig. 5(a), and the rods R_{s1} and R_{s2} are optimized to 48 nm and 30 nm, respectively. The overall size of the waveguide used as NOT gate is same as the size of the waveguide

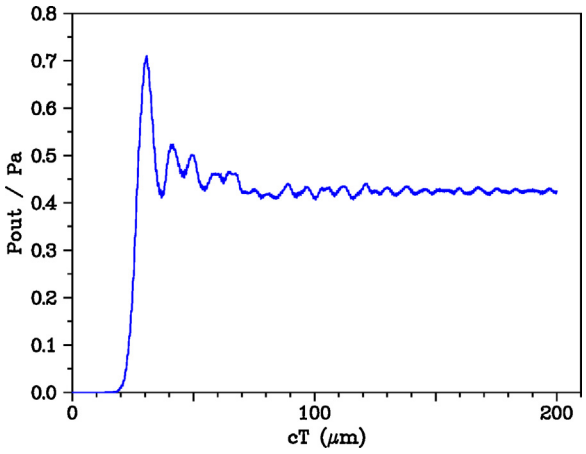


Fig. 7. Time evolving curve from the proposed NOT gate.

used as XOR gate which was presented in the previous subsection. This gate is same as that of the reported NOT gate [22], but the operation of it differs when it is being cascaded with respect to the input phase variation. It consists of an input port *A* along with the additional port to apply the reference input REF, and an output port *Y*. As the structural parameters such as radius of the normal rod, lattice-type, lattice constant, as well as the refractive index of each rod are same as that of the proposed XOR gate this logic gate structure also offers the same PBG's.

The rod R_{s1} is optimized to 48 nm at which the output transmission is above 0.4 with low reflection as shown in Fig. 5(b). In this logic gate structure, when input *A* is not excited, the reference input acts as an output. When input *A* is excited then it should be nullified so as to produce a very low light intensity at the output as logic '0'. In order to achieve this, reference input is applied with 180° phase and input *A* with zero phase. Thus, a destructive interference occurs at the junction due to 180° phase difference and the output port *Y* will get a very low or negligible light intensity which can be read as logic '0'. In both the input conditions of the NOT gate the reference input is always maintained at 180° phase.

Simulation on the proposed NOT gate has been carried out with respect to the input conditions, and results are analyzed in the same manner as in the previous case. The electric field distribution in the structure upon applying the input is shown in Fig. 6. According to the figure, when input port *A* is not excited, the reference input turns towards the output port *Y*, and provides an output transmission of 0.4255 which can be read as logic '1'. When the input port *A* is excited with the light signal, the reference input will interfere destructively with that signal as they are out of phase with each other at the same path lengths. As a result of which, a very low or negligible transmission of 0.0000014 is observed at port *Y*. This negligible transmission of logic '0' can be observed from Fig. 6(c) wherein the steady state response is shown, which is being considered as the power level of logic '0'. This negligible value of the output intensity is achieved because of the perfect destructive interference occurs between the inputs due to symmetric excitation. Thus, the proposed structure acts as a NOT gate due to out of phase inputs. The ON to OFF contrast ratio is calculated from these values, and it is 54.83 dB which is also higher than the existing NOT gates available in the literature. This type of symmetric input excitation can very well be observed in the NOT gate designed with rectangular shaped waveguide [31] which has also been reported with higher contrast ratio.

The response time is calculated from the time evolving curve obtained from the NOT gate structure which is shown in Fig. 7. The time (T) required to reach 90% of P_{avg} is of 0.0874 ps (cT = 26.2 μm) with t_{11} = 0.056 ps (cT = 16.8 μm) and t_{12} = 0.0314 ps (cT = 9.4 μm). Thus, a narrow pulse of width 0.0628 ps can be produced which leads to a response time of 0.1256 ps. Table 2 gives the summary on the output performance of the proposed NOT gate.

Table 2
Output performance of the proposed NOT gate.

Input	Output (*Y*)			
A	Transmission (P_{out}/P_a)	Logic	Contrast ratio	Response time
0	0.4255	1	54.83 dB	0.1256 ps
1	0.0000014	0		

3. Realization of all-optical XNOR gate

As it was discussed in the previous section, the cascading of XOR gate with NOT gate derives the XNOR logic function. In this section, the proposed XOR and NOT gates are cascaded to derive the XNOR logic function. But instead of connecting the output Y_1 of XOR gate with the input *A* of NOT gate, they are superimposed as shown in Fig. 8 in order to decrease the size of the realized structure. In the proposed XOR and NOT gates, the lengths of waveguide's input branches (*A* and *B* in XOR gate, and *A* and REF in NOT gate) are kept same in order to have a perfect interference between the input signals. Similarly, in the proposed XNOR structure also, the path length of the reference input to reach the junction of NOT gate section should be same as that of the path length of the light from the input (*A* or *B*) of the XOR gate to the junction of NOT gate section for the inversion (NOT) operation to happen. Thus, the length of the reference input waveguide is extended such that the path length for the reference light can be equal to the path length of the light from the port *A* or port *B*. Moreover, this waveguide extension assures same number of bends for the light signals to reach the junction from both the input sides (*A* and/or *B* and reference input) so as to have a perfect interference. Further, three additional rods R_e along with two R_{s2} rods are introduced in the extended waveguide which have the same radius as that of R_a to counter balance the effect of the additional rods of XOR gate section.

The reference input in the NOT gate is responsible to invert the input, and as it was discussed earlier, its phase plays a vital role in the inversion. The reference input is taken such that the phase difference with the input *A* should be of 180°. In the proposed XNOR functional structure, the phase of the reference input is changed with respect to the input of the XOR gate as its inputs (*A* and *B*) are out of phase. The phase of the reference input is maintained at 180° for all the input combinations shown in the truth table of Fig. 1(a) except for the second one, to which it is 0° (because input port *B* is excited with a 180° phase). When ports *A* and *B* are not excited, the reference input will reach port *Y* as logic '1'. Similarly, when both ports *A* and *B* are excited with light signals, they will interfere destructively and a very negligible light intensity reaches to both the junctions of XOR and NOT gate sections, and, thus the reference signal directs toward output *Y* as logic '1'. When port *A* is only excited with light signal, the reference input will interfere destructively with it at the junction of NOT gate section and produces a low intensity which is read as logic '0'. Similar operation happens when only port *B* is excited due to phase change of the reference input.

Simulation has been carried out on the proposed XNOR gate for all the four input combinations, and results are analyzed to calculate the contrast ratio and the response time. The electric field distribution in the proposed XNOR gate for all the four input combinations is shown in Fig. 9. When the input ports are not excited, the reference input diverts towards the output port *Y* and provides a transmission of 0.412 which is read as logic '1'. Later, upon the

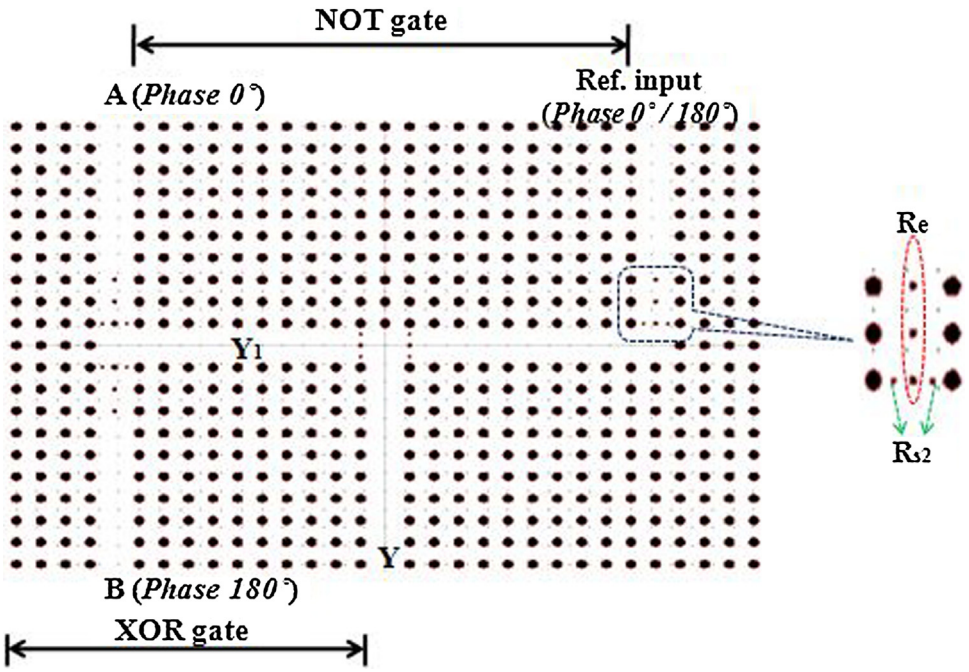


Fig. 8. Lattice structure for the realization of XNOR logic function.

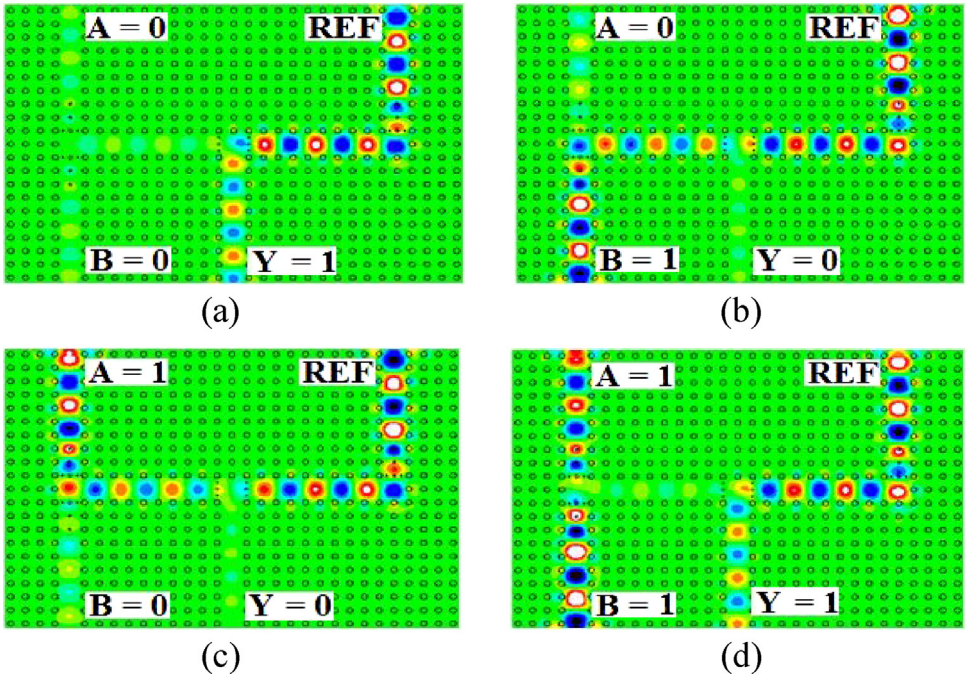


Fig. 9. Electric field distribution of the structure of realized XNOR function for inputs a) A = 0, B = 0, b) A = 0, B = 1, c) A = 1, B = 0, and d) A = B = 1.

excitation of only port *A* with the light signal, the reference input will get destructively interfered with it at the junction of NOT gate due to phase difference of 180° and provides an output transmission of 0.0244 at port *Y*, and it is read as logic '0'. Similar operation happens when only *B* is applied due to phase change of reference input, and the same output transmission of 0.0244 is observed at port *Y* which is read as logic '0'. When both the ports *A* and *B* are excited with out of phase input light signals, destructive interference at the first junction allows the reference input to reach the port *Y*, and provides a transmission of 0.412, which is read as logic '1'. The calculated value of the contrast ratio based upon the achieved results is of 12.27 dB.

Similar to the previous section, the response time is calculated from the time evolving curve observed from the proposed XNOR structure, and is shown in Fig. 10. The time (T) required to reach 90% of P_{avg} is 0.134 ps (cT = 40.2 μm) which consists of two components t_{11} = 0.0944 ps (cT = 28.3 μm) and t_{12} = 0.0397 ps (cT = 11.9 μm). Thus, a narrow pulse of width of 0.0794 ps can be produced which leads to a response time of 0.1588 ps. Summary on the output performance of the realized XNOR gate is given in Table 3. On comparing the response time of the proposed XNOR gate with the XOR and NOT gates, it can be concluded that the response time of the XNOR gate increases due to the cascading. This delay in the response of XNOR gate structure can well be described from the

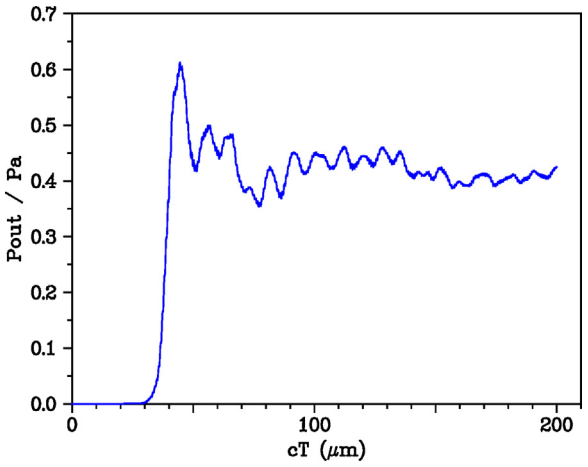


Fig. 10. Time evolving curve from the structure of realized XNOR function.

Table 3
Output performance of the structure of realized XNOR function.

Input		Output (*Y*)			
A	B	Transmission (P_{out}/P_a)	Logic	Contrast ratio	Response time
0	0	0.412	1	12.27 dB	0.1588 ps
1	0	0.0244	0		
0	1	0.0244	0		
1	1	0.412	1		

transmission delay t_{11} values of all the three logic gates. It shows that the transmission delay is more for XNOR gate, and this is due to cascading of XOR gate with NOT gate. The performance of the XNOR structure is constant over the C-band (1530 nm–1565 nm) as shown in Fig. 11. The output transmission for logic '0' and logic '1' used to calculate the contrast ratio is constant over the entire C-band as illustrated by Fig. 11(a). Obviously, these values will lead to the contrast ratio which is also same all over the band as shown by Fig. 11(b). There is a negligible variation in the transmission over this band which does not have effect on the contrast ratio.

Finally, with respect to the overall performance of the proposed structure of XNOR logic function, it can be concluded that the cascading of all-optical logic gates which based on interference provides considerable results. But, there needs to improve the parameters such as contrast ratio further, so that the performance of the realized structure can be comparable with the logic gates which are instantiated (in this case proposed XOR and NOT gates). This becomes possible whenever the destructive interference in the realized structure provides a lower or negligible intensity at the output as logic '0'. Because, as low as the power level of logic '0' is, the higher will be the contrast ratio. Advancements in the material characteristics in this sense can make this true which may lead these all-optical designs to be competent to the electronic counterparts in all aspects of high speed optical computing and telecommunication systems.

4. Comparison with logic gates based on Y-shaped, cross shaped and rectangular shaped waveguides

The proposed work is compared with the logic gates existing in the literature so far which were designed with Y-shaped [23,24], cross shaped [13,20] and rectangular shaped waveguides [31]. The comparison has been done on all the logic gates with respect to the contrast ratio and response time. The main aim of the proposed NOT and XOR gates is to check the possibility of their cascading with acceptable performance and compact size. Thus, apart from comparing the cascaded XNOR gate with the existing XNOR gates in the literature, the improvement in size due to cascading has also been compared with the two gate cascaded structure [26]. Table 4 gives a complete summary on the comparison with respect to structural variation, contrast ratio and response time.

From Table 4, it can be concluded that the photonic crystal based T-shaped waveguide with symmetric input excitation leads to higher contrast ratio whether it is XOR gate or NOT gate. In the NOT gate, the input excitation is symmetric, and, thus a perfect destructive interference occurs at the junction of the T-shaped waveguide due to 180° phase difference. This is the basic reason to produce negligible intensity as logic '0'. This negligible intensity as logic '0' leads to higher contrast ratio, and as compared with the existing gate [31] it is improved by more than twofold. The symmetric input excitation can very well be observed in the NOT gate designed with rectangular shaped waveguide [31] which has also been reported with higher contrast ratio. But, the size, as well as the resonance dependent phenomenon made the gate [31] to be inferior to the proposed NOT gate. In contrast, the asymmetric excitation of the T-shaped waveguide based NOT gate with point defect at the edge [21] leads to higher contrast ratio compared with the other reported gates [23,24] but far less than the proposed NOT gate. The similar case of asymmetric excitation can also be observed in the gate [13] with admirable contrast ratio but lesser than the proposed one.

The same excitation pattern (as in the proposed NOT gate) is observed in the proposed XOR gate which has made it superior in terms of contrast ratio over the existing XOR gate designed with Y-shaped [23,24] and cross-shaped waveguides [20]. The contrast ratio of the proposed XOR gate is improved by 1.53 times than the

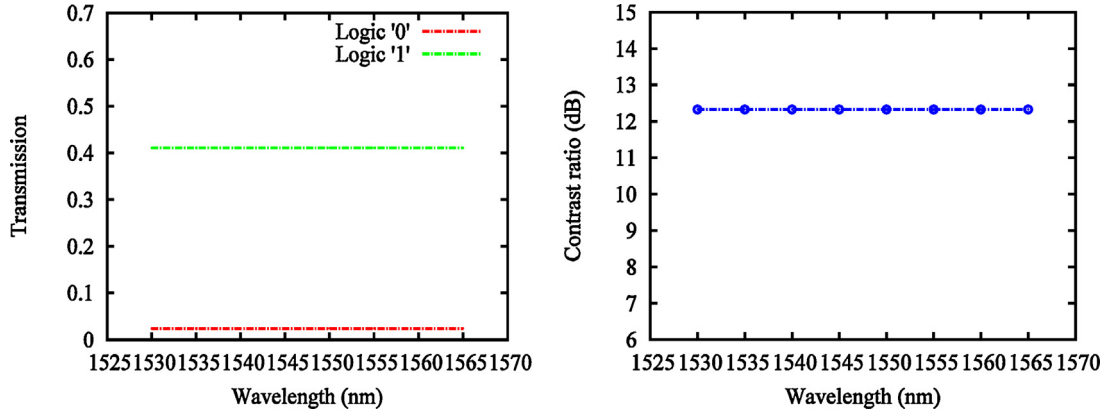


Fig. 11. Performance of the structure of realized XNOR function over C-band a) output transmission for logic '0' (red) and logic '1' (green) and b) contrast ratio.

Table 4
Comparison with the exiting logic gates designed with different types of waveguides.

Logic gates reported in the literature	Structural characteristics	Type of the gates	Contrast ratio (dB)	Response time (ps)
Wu et al., 2012 [13]	Cross shaped waveguide with square-type lattice	NOT	24.73	0.464
Rani et al., 2015 [23]	Y-shaped waveguide with triangular-type lattice	NOT	5.42	1.024
		XOR	8.49	
		XNOR	5.42	
Nirmala et al., 2016 [31]	Rectangular shaped waveguide with square-type lattice	NOT	35.97	–
		XOR	35.97	
Kiyanoosh et al., 2016 [20]	Cross shaped waveguide with square-type lattice	XOR	6.767	0.4
Rani et al., 2017 [24]	Y-shaped waveguide with triangular-type lattice	NOT	3.74	2.168
		XOR	6.50	
		XNOR	6.50	
Proposed work	T-shaped waveguide with square-type lattice	NOT	54.83	0.1256
		XOR	55.23	0.1360
		XNOR	12.27	0.1588

existing. Although the proposed XNOR gate is the cascaded version of NOT and XOR gates, the contrast ratio is higher by twofold than the Y-shaped waveguide [23,24]. As far as the response time of all the three proposed gates is concerned, it is decreased by more than 60.3%.

The area occupancy of the cascaded XNOR gate is calculated with respect to the basic gate structures (XOR and NOT). The size of XOR and NOT is of 12.24 μm × 8.64 μm and 8.64 μm × 12.24 μm, respectively. As the cascading of the basic gates is done by superimposing the output branch of the waveguide of XOR gate (port Y_1) with the input branch of the waveguide of NOT gate (port A), the size of the cascaded structure becomes 12.24 μm × 18.24 μm. From these values, it can be observed that, the area occupancy from basic to cascaded structure is increased by 111%. When it is compared with a two gate cascaded structure proposed by T. A. Moniem *et al.*, [26], it can be concluded that the area occupancy of the proposed XNOR gate due to cascading is lowered by a factor of 3.19. This shows the compactness of the proposed basic and cascaded logic gate designs, and also the less complexity incurred in the cascading of T-shaped waveguide based logic gates.

5. Conclusions

We proposed high contrast all-optical XOR and NOT logic gates on a 2D photonic crystal of square-type lattice, and they are cascaded to realize the XNOR logic function. T-shaped waveguides have been used to design these gates, and for an inversion operation in the NOT gate an extra input is used namely reference input. In both the gates, the inputs are applied with out of phase in order to have a perfect destructive interference to produce low output power for logic '0'. This low power level of logic '0' has improved the output contrast ratio drastically in both the gates, and they have been resulted with the contrast ratio of above 50 dB at a response time of below 0.2 ps. Finally, these two gates have been cascaded by superimposing the output branch of the waveguide of XOR gate with the input branch of the waveguide of NOT gate to realize the XNOR logic function. Besides the compact size, the final structure designed for the realization of XNOR logic function has achieved a contrast ratio of 12.27 dB at a response time of 0.1588 ps.

Acknowledgement

Enaul haq Shaik is thankful to University Grants Commission, India for providing financial support through UGC-MANF Fellowship.

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