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A zero-voltage-switching current source inverter with three-stage space vector modulation for low-input voltage stand-alone applications

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Abstract: In this paper, a three-stage space vector pulse width modulation (SVPWM) along with soft switching is proposed for a high-voltage transfer ratio single-stage three-phase current-source inverter (HVTR-CSI) to reduce switching losses and improve inverter efficiency. The proposed SVPWM strategy utilizes the conduction state of the energy storage switch as the zero vector and assigning effective vectors action modes. The zero-voltage-switching (ZVS) of the energy storage switch is achieved by resonant parameters and controlling the turn-on time of the active clamp circuit. The circuit topology, operation principle, high-frequency switching process of the studied CSI are thoroughly analyzed, and detailed calculations of the circuit parameters and soft-switching design are performed. Experimental results on a 1 kW 24 VDC/84 VAC 3-phase AC prototype show that the modulation improves the CSI peak efficiency by 1.15% compared to sinusoidal pulse width modulation (SPWM). This study provides an effective design approach for the HVTR-CSI in terms of reducing switching losses.

Key words: boost voltage ratio, current source inverter (CSI), three-stage SVPWM strategy (SVM), zero voltage switching (ZVS)

1. Introduction

In outdoor camping and vehicle applications, low-voltage batteries are commonly used to power various devices in order to achieve lightweight batteries, while large devices such as electric ovens, sound systems, and power tools require three-phase high-voltage AC power [1–3]. Typically,

a DC–DC boost stage is incorporated between the battery and the inverter to achieve voltage matching between input and output. Such the two-stage inverter system offers the advantage of flexible control strategies but suffers from drawbacks including complex structure, increased cost, low reliability and low conversion efficiency [4, 5]. To reduce the size, weight, and cost of such inverters and improve the conversion efficiency, researchers have carried out studies on boost inverters such as Z-source inverters (ZSIs) and current-source inverters (CSIs), aiming to achieve high power density, high voltage transfer ratio, and high conversion efficiency.

ZSIs and quasi-ZSIs have been proposed in References [6, 7]. These inverters utilize unique DC-link impedance networks and the straight-through operation of the impedance branches to achieve high voltage boost. However, the voltage gain of such inverters is limited because the boost ratio and modulation ratio are coupled, resulting in a decrease in the modulation index when the voltage gain is increased [8]. Some studies have focused on new structures of ZSIs with high voltage gain. In [9], a switched inductor ZSI (SL-ZSI) was proposed, where the impedance elements are replaced with switched inductors, thereby enhancing the voltage boost capability of the ZSI. A tapped inductor Z-source inverter (TL-ZSI) was proposed in paper [10] to achieve high voltage boost by varying the turns ratio of the coupled inductors.

In [11], a switch capacitor ZSI (SC-ZSI) was introduced, where impedance elements are replaced with switched capacitors. In [12], an enhanced boost-type ZSI was proposed, which utilizes the cascaded connection technique to assemble lower-rated components. These approaches modify the impedance network to increase the boost ratio of the inverter. However, this leads to a complex impedance network, larger passive component volume, and reduced reliability and conversion efficiency of the ZSI.

Compared to two-stage DC–AC inverters, the CSI offers the advantages of single-stage boost inversion and high-quality output waveform. Furthermore, compared to the ZSI topology family, the CSI requires only energy storage inductors for boost without the need for complex impedance networks, resulting in a smaller size and lower cost. Therefore, the CSI is more suitable for low-voltage single-stage boost inverter applications. However, the traditional CSI suffers from limitations such as low boost capability and low conversion efficiency. To enhance the boost capability of the CSI, a coupled inductor-based CSI was proposed in [13] to achieve high voltage gain. However, it has the drawbacks of complex boost unit structure and low efficiency. The single-stage three-phase CSI with a low-voltage transfer ratio (VTR) proposed in References [14, 15] exhibits advantages such as single-stage power conversion and boost characteristics. However, it still has defects, such as an insufficient voltage transfer ratio, and the output waveform quality and conversion efficiency are seriously affected when the input voltage is too low or the input voltage variation range is too wide. Therefore, to overcome the limitations of the aforementioned CSI in terms of single-stage boost, power density, and conversion efficiency, a high-voltage transfer ratio single-stage three-phase CSI (HVTR-CSI) was proposed in [16], as shown in Fig. 1.

Additionally, it employs an improved zone sinusoidal pulse width modulation (SPWM) strategy and an active clamp branch circuit. Due to the introduction of the clamp circuit, the turn-off voltage spikes of the energy storage switch can be suppressed. However, a drawback of the modulation scheme in the paper is that the zero-vector acts twice, leading to a higher number of switching operations for the energy storage switch S and clamp switch SC, without implementing soft switching to reduce switching losses. Space vector modulation (SVM) provides a new way to generate gating signals for current-based inverters. Compared with sine pulse width modulation

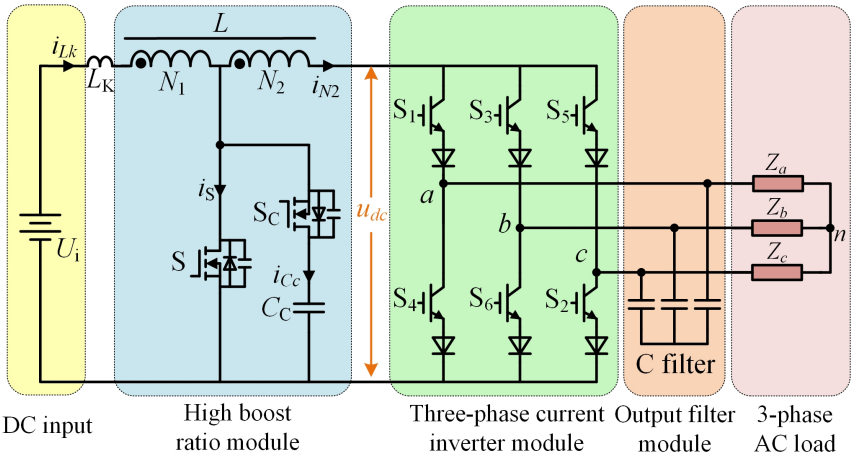


Fig. 1. Configuration of the studied ZVS-CSI

(SPWM), SVPWM not only achieves higher voltage gain, but also meets the needs of more complex control by selecting different space vectors, adjusting the action time of these vectors, and optimizing the sequence of vector actions, enabling the system to achieve more precise and flexible control according to specific application requirements more precise and flexible control [17, 18]].

In this paper, a new three-stage space vector pulse width (SVPWM) technique is proposed for the HVTR-CSI and a soft-switching implementation of ZVS is investigated. Three-stage SVPWM enables S and SC to be turned on and off only once within a single high-frequency switching cycle, which can effectively reduce the switching losses of S, and the switching losses are further reduced by soft-switching to improve the inverter. The rest of this paper is organized as follows: the three-stage SVPWM strategy and the analysis of the ZVS high-frequency operation mode of the CSI are presented in Section 2. Then, the CSI parameter design and the conditions for implementing soft-switching are described in Section 3. The experimental results are demonstrated in Section 4. Finally, the conclusion is provided in Section 5.

2. Modulation strategy and operation modes

2.1. Modulation strategy

In this paper, a new three-stage SVPWM strategy is constructed for the CSI under study. The special feature of this method is that the conduction of the switch S is used as the zero vector, replacing the conduction of the inverter bridge arm. Taking sector I as an example, the modulus I_{ref} of the reference current vector is at an angle θ to the α coordinate axis, and the total time of sector I is $T_s I_{\text{ref}}$ is synthesized by two adjacent effective current vectors I_1 and I_2, whose vectors act at times T_1 and T_2, respectively. Additionally, the zero vector I_0 should be included, and its action

time is defined as T_0. The relationship between I_{ref} and the current vector is shown in Eq. (1):

$$T_0 \times \boldsymbol{I}_0 - \mathrm{j}T_1\boldsymbol{I}_1 + T_2\left(\frac{\sqrt{3}}{2} - \mathrm{j}\frac{1}{2}\right)\boldsymbol{I}_2 = T_S\boldsymbol{I}_{\mathbf{ref}} = T_S\boldsymbol{I}_{\mathbf{ref}}e^{\mathrm{j}\theta}. \tag{1}$$

The action times of vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_2$ are given by Eq. (2) where I_{dc} is the DC bus current vector. The other sectors are calculated in the same way as sector I. i_α and i_β are the components of the current vector transformed to the $\alpha - \beta$ axis system.

$$\begin{cases} T_1 = -\dfrac{T_S I_{\text{ref}} \cos(\theta)}{2I_{dc}} - \dfrac{\sqrt{3}T_S I_{\text{ref}} \sin(\theta)}{2I_{dc}} \\ T_2 = \dfrac{T_S I_{\text{ref}} \cos(\theta)}{I_{dc}} \end{cases}. \tag{2}$$

To simplify the calculation, the effective vector action time of each sector can be expressed by the two values in Eq. (3), so in the SVPWM calculation process, the three values in Eq. (3) are firstly calculated based on the currentsi_α and i_β, which are set as X, Y, and Z, and then called according to the selection of the sector in which I_{ref} is located, which can further simplify the process of calculating the vector action time of the sector. The switch states corresponding to the three-phase currents form current vectors, and the spatial positions of the current vectors $I_1 - I_6$ in the $\alpha - \beta$ coordinate system are shown in Fig. 2.

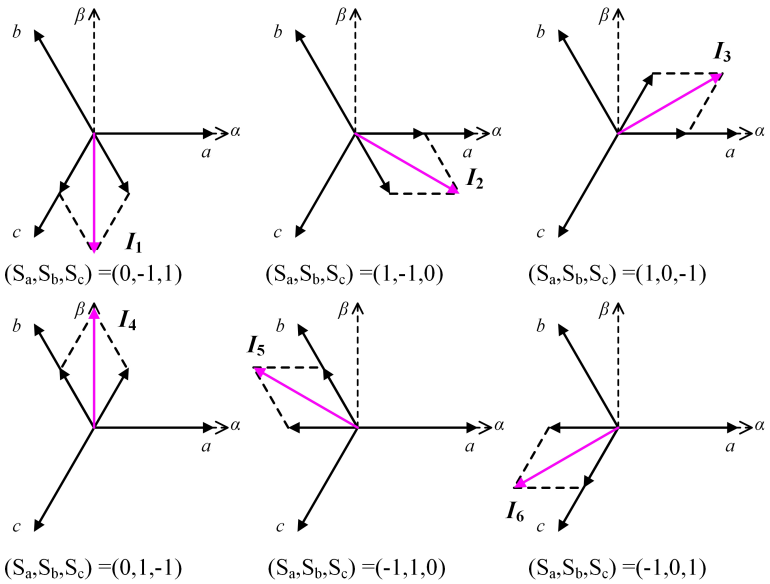


Fig. 2. Current vector space position

$$\begin{cases} X = \dfrac{T_S I_{\text{ref}} \cos(\theta)}{I_{dc}} = \dfrac{T_S}{I_{dc}} i_\alpha \\ Y = \dfrac{T_S I_{\text{ref}} \cos(\theta)}{2I_{dc}} + \dfrac{\sqrt{3} T_S I_{\text{ref}} \sin(\theta)}{2I_{dc}} = \dfrac{T_S}{2I_{dc}} (i_\alpha + \sqrt{3} i_\beta) \\ Z = -\dfrac{T_S I_{\text{ref}} \cos(\theta)}{2I_{dc}} + \dfrac{\sqrt{3} T_S I_{\text{ref}} \sin(\theta)}{2I_{dc}} = \dfrac{T_S}{2I_{dc}} (-i_\alpha + \sqrt{3} i_\beta) \end{cases} . \tag{3}$$

According to the three-stage SVPWM principle, the action time of the zero vector can be expressed as $T_S/2 - T_1 - T_2$. After determining the action time of the three vectors in each sector, the output current can be modulated by controlling the on-off of the switch S and the inverter bridge arm switches S_1–S_6. In the SVPWM calculation process, the matched vector action times T_1 and T_2 can be selected directly by the sector in which they are located according to Table 1.

Table 1. Time of sector vector actions

Sector	**I**	**II**	**III**	**IV**	**V**	**VI**
T_1	$-Y$	$-Z$	X	Y	Z	$-X$
T_2	X	Y	Z	$-X$	$-Y$	$-Z$

To achieve ZVS of S, an active clamp circuit needs to be added. The general sector switch sequence for the CSI is shown in Fig. 3.

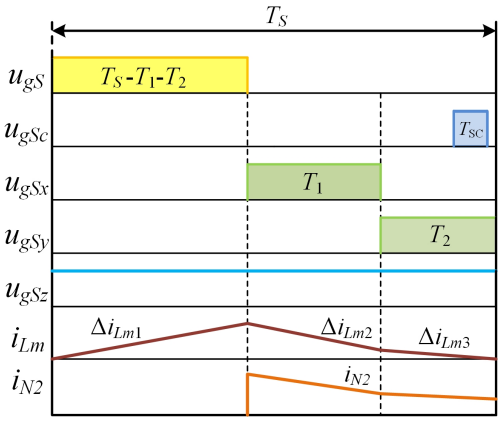


Fig. 3. Switching sequences of ZVS-CSI

During the three-stage SVPWM process, the variation of the equivalent excitation inductor current follows the pattern of rising during the T_0 time period and falling during the T_1 and T_2 time periods, corresponding to the energy dissipation of the inductor during the action of the effective current vectors. The switching sequence of the current vectors within and between different sectors is shown in Fig. 4.

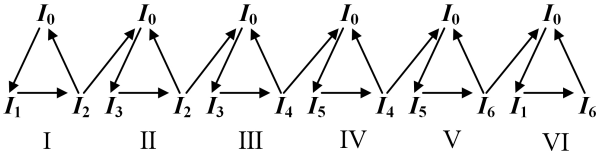


Fig. 4. Three-stage modulation mode vector switching sequence

2.2. Analysis of Operation modes

Taking sector I as an example, the circuit waveforms during the key high-frequency cycle of the studied CSI are shown in Fig. 5. Additionally, the equivalent modal circuits for each period are shown in Fig. 6. During this stage, S_6 is always ON, while S_2, S_3 and S_4 are OFF. The synthesis of the current vector I_{ref} is controlled by controlling the on-time of switches S, S_1 and S_5. The following is a detailed analysis of the operating mode of sector I.

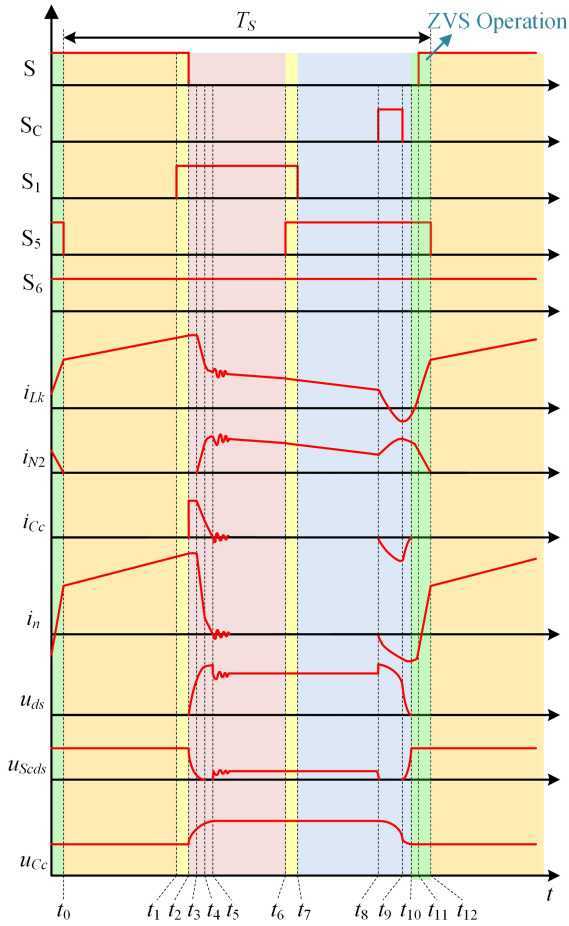


Fig. 5. Key waveforms in sector I

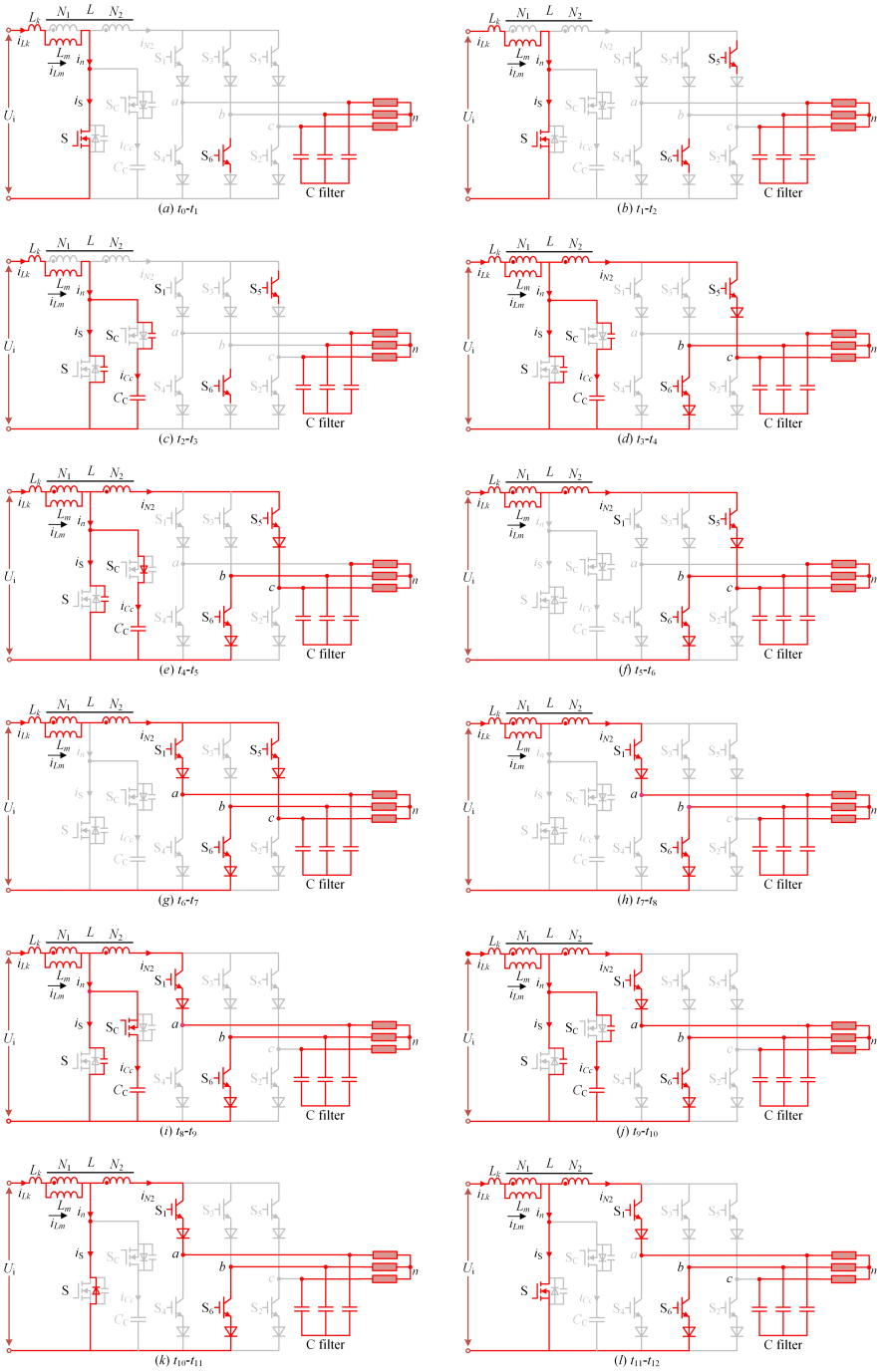


Fig. 6. Working modes in sector I

1. *Mode 0* ($t_0 - t_1$): Charging of the N_1 winding
   Before time t_0, S has been turned on. When the current of the N_2 winding drops to 0, *Mode 0* begins. During *Mode 0*, the excitation inductor L_m consisting of the N_1 winding, starts to magnetize. The variation of the excitation inductor current i_{Lm} can be expressed by the following Eq. (4):
   $$U_i = (L_m + L_k)\frac{\mathrm{d}i_{Lm}}{\mathrm{d}t}, \tag{4}$$
   where: U_i is the input voltage, L_k is the leakage inductor of the circuit, and i_{Lm} is equal to the leakage inductor current i_{Lk}.
2. *Mode 1* (t_1–t_2): Turning on energy release switch S_1
   Before S is turned off, it is necessary to turn on the switch S_1 for a short time as a dead time due to the dual relationship between the CSI and VSI. Then, when the switch S is opened, it provides a freewheeling path for the inductor current.
3. *Mode 2* (t_2–t_3): Turning off energy store switch S
   Mode 2 starts when the switch S is turned off, at which points i_{Lk} and i_{Lm} cannot be mutated. Therefore, the parasitic capacitance of the switch S and S_C are charged by i_{Lk}, and the drain-source voltage of S increases rapidly. At the same time, the drain-source voltage of the switch S_C drops rapidly.
4. *Mode 3* (t_3–t_4): Starting the release of energy to the load
   When u_{dc} is higher than the line voltage at the output, $i_{N\ 2}$ in the N_2 winding starts to increase from zero. C_{oss} is neglected since it is much smaller than C_C. At this stage, due to the characteristics of C_C and L_k, resonance starts.
5. *Mode 4* (t_4–t_5): Resonance stage
   The resonant charging process of the capacitor C_C begins in *Mode 3*, but *Mode 3* is very short-lived. Therefore, the resonant charging mainly occurs in *Mode 4*. The circuit equations for the resonance process between C_C and the inductor are as follows, Eq. (5):
   $$\begin{cases} i_n = i_{Lk} - i_{N2} \\ i_{Cc} = \dfrac{C_C}{C_{oss} + C_C} i_n \approx i_n \\ i_{Cc} = C_C \dfrac{\mathrm{d}u_{Cc}}{\mathrm{d}t} \\ u_{N2} = u_{Cc} - u_{ab} \\ u_{Lm} = u_{N1} = \dfrac{N_1}{N_2} u_{N2} \\ U_i = L_k \dfrac{\mathrm{d}i_{Lk}}{\mathrm{d}t} + \dfrac{N_1 + N_2}{N_2} u_{Cc} - \dfrac{N_1}{N_2} u_{ab} \\ i_{Lk} = i_{Lm} + i_{N1} = i_{Lm} - \dfrac{N_2}{N_1} i_{N2} \end{cases}, \tag{5}$$
   where: i_{Cc} is the clamp capacitor current, u_{ab} is the line voltage between output phase a and phase b, u_{N1} and u_{N2} are the voltages across the N_1 and N_2 windings, respectively. At this stage, the current i_{N2} in the N_2 winding starts to drop and the inductance of L_m is equal to L_1.

6. *Mode 5* (t_5–t_6): Releasing energy stage.
   At this stage, the input power supply U_i and the inductor L are simultaneously output to the load, and i_{N2} is equal to i_{Lk}. The equation for i_{Lk} can be expressed as Eq. (6):
$$(U_i - u_{ab})\left(\frac{N_1}{N_1 + N_2}\right)^2 = L_m \frac{\mathrm{d}i_{Lk}}{\mathrm{d}t}. \tag{6}$$
   At the beginning of this stage, the leakage inductance L_k and the parasitic capacitance of the *metal–oxide–semiconductor field-effect transistor* (MOSFET) will undergo a short resonant process.
7. *Mode 6* (t_6–t_7): Turning on switch S_5
   Mode 6 means the starting of the second vector. In order to ensure the dead zone, S_5 needs to be turned on before S_1 is OFF.
8. *Mode 7* (t_7–t_8): Turning off switch S_1
   Mode 7 starts with turning off S_1 after the dead zone. During this stage, Eq. (6) can be changed as (7):
$$(U_i - u_{cb})\left(\frac{N_1}{N_1 + N_2}\right)^2 = L_m \frac{\mathrm{d}i_{Lk}}{\mathrm{d}t}. \tag{7}$$
9. *Mode 8* (t_8–t_9): Turning on clamp switch S_C
   Mode 8 starts when S_C is turned on. u_{Cc} is higher than the voltage at the center-tap of the inductor L, therefore, the voltage u_{Lk} across L_k is negative. At this time, the voltage across L_k is as shown in Eq. (8):
$$u_{Lk} = L_k \frac{\mathrm{d}i_{Lk}}{\mathrm{d}t} = U_i - \frac{N_1 + N_2}{N_2} u_{Cc} + \frac{N_1}{N_2} u_{cb}. \tag{8}$$
   The current i_{Cc} increases in the reverse direction from zero and C_C releases energy to the leakage inductance L_k.
10. *Mode 9* (t_9–t_{10}): Turning off clamp switch S_C
    To achieve zero-voltage turn-on of S, S_C is turned off before the resonance current starts to decrease. Then, the current i_{Lk} is continuously wheeling. The drain-source voltage of S rapidly decreases to zero due to the discharge of its parasitic capacitance.
11. *Mode 10* (t_{10}–t_{11}): ZVS realization
    Mode 10 starts when the drain-source voltage u_{ds} of S drops to zero. At this point, S can achieve ZVS. Because the higher current at the input leads to higher current stress in S, ZVS can significantly reduce switching losses.
12. *Mode 11* (t_{11}–t_{12}): Turning on switch S
    Before the energy storage switch branch circuit current i_S reverses and decreases to zero, S is turned on. During this period, the current i_S initially decreases in the reverse direction and then increases in the forward direction. At the same time, the current in the N_1 winding rapidly increases, while the current in the N_2 winding rapidly decreases until it reaches zero.

3. Circuit design and analysis of ZVS operation

In this paper, the rated output power P_O of the studied CSI is 1 kW. The input voltage U_i is 24 V, and the three-phase phase output voltage RMS value U_N is 84 V. The switching frequency of the CSI is 50 kHz.

3.1. Design of power circuits

For the high-frequency coupled inductor parameter design, within one steady-state high-frequency switching cycle, neglecting the effects of parasitic parameters such as leakage inductance, switching parasitic capacitance, and stray capacitance of the inductor primary and secondary inductors, the inductor L stores energy once and releases it twice, and thus the ideal equivalent circuit of the inductor L can be obtained as shown in Fig. 7(a). Meanwhile, the switching waveforms of the excitation inductance current i_{Lm}, the primary inductance current i_{N1} and the secondary inductance current i_{N2} in one steady-state high-frequency cycle are obtained as shown in Fig. 7(b).

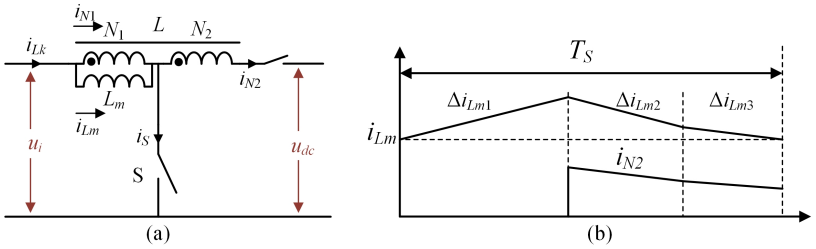


Fig. 7. Inductor parameter analysis: (a) ideal equivalent circuit of inductor; (b) ideal waveform of current for high frequency switching cycle

In the Δi_{Lm1} stage, the excitation inductor current i_{Lm} increases linearly with an increment of Δi_{Lm1}, in which both i_{N1} and i_{N2} are constant zero, and in the Δi_{Lm2} stage, the excitation inductor current i_{Lm} decreases linearly with a negative increment Δi_{Lm2}, and in this stage, i_{N1} and i_{N2} can be expressed as Eq. (9). The Δi_{Lm3} stage has basically the same principle as the Δi_{Lm2} stage, where the excitation inductor current i_{Lm} decreases linearly, but the slope of the decrease is different.

$$\begin{cases} i_{N1} = -i_{Lm}\dfrac{N_2}{N_1+N_2} \\ i_{N2} = i_{Lm}\dfrac{N_1}{N_1+N_2} \end{cases}, \tag{9}$$

where Δi_{Lm1}, Δi_{Lm2}, and Δi_{Lm3} corresponding to vector action times of T_0, T_1, and T_2, respectively, can be expressed as Eq. (10):

$$\begin{cases} T_1 = -\dfrac{T_S}{2I_{dc}}(i_\alpha + \sqrt{3}i_\beta) \\ T_2 = \dfrac{T_S}{I_{dc}}i_\alpha \\ T_0 = T_S - T_1 - T_2 \end{cases}. \tag{10}$$

Taking sector I as an example, the relationship between the duty of the active vectors D_1, D_2 and the unit sine functions e_a and e_c is as follows in Eq. (11):

$$\begin{cases} D_1 = Ke_c \\ D_2 = Ke_a \\ D_0 = 1 - D_1 - D_2 \end{cases}, \tag{11}$$

where D_1 and D_2 are $T_1/(T_S/2)$ and $T_2/(T_S/2)$, respectively, and T_S is one switching cycle. K is the modulation coefficient. As shown in Fig. 5, the inductor L is charged and discharged twice in one switching cycle. The two charging cycles are T_1 and T_2, respectively. The inductor current change increments can be expressed in T_S. Then, the incremental change of excitation inductor current can be obtained by a high-frequency steady-state analysis and vector action time calculation as in Eq. (12):

$$\begin{cases} \Delta i_{Lm1} = \dfrac{U_i}{L_m}(1 - D_1 - D_2)T_S \\ \Delta i_{Lm2} = \dfrac{(U_i - u_{cb})\dfrac{N_1}{N_1 + N_2}}{L_m} D_1 T_S \\ \Delta i_{Lm3} = \dfrac{(U_i - u_{ab})\dfrac{N_1}{N_1 + N_2}}{L_m} D_2 T_S \end{cases}. \tag{12}$$

According to the principle of inductor volt-second balance, the inductor current changes by zero during a switching cycle. In addition, the relationship between the output line voltage and the unit sine function can be expressed by the following Eq. (13):

$$e_a u_{ab} + e_c u_{cb} = \frac{3}{\sqrt{2}} U_N \cos(\theta) = \frac{3}{\sqrt{2}} U_N, \tag{13}$$

where U_N is the RMS output phase voltage and θ represents the angle of the power factor. The voltage transfer ratio can be obtained by solving Eqs. (12) and (13), The voltage transfer ratio can be expressed by Eq. (14) as:

$$\frac{U_N}{U_i} = \frac{N_1 + N_2}{N_1} \frac{2\sqrt{2}}{3K\cos(\theta)} - \frac{N_2}{N_1} \frac{\sqrt{2}(e_A + e_C)}{3\cos(\theta)}. \tag{14}$$

The peak value of the output phase current is expressed in Eq. (15):

$$\sqrt{2} I_p = \frac{N_1}{N_1 + N_2} \frac{K I_{Lavg\,\max}}{2} = \frac{\sqrt{2} P_o}{3 U_N \eta}, \tag{15}$$

where the coefficient η represents the conversion efficiency of the CSI, and $I_{Lavg\,\max}$ is the peak constant current at a steady state. P_O is the output power. If he input current ripple is less than 15% under full load conditions, then Eq. (16) is as follows:

$$\frac{\Delta i_L}{i_L} = \frac{U_i}{L_1 I_{Lavg\,\max}}(1 - D_{\min})T_S \le 0.15. \tag{16}$$

From this, it can be concluded that the value of the excitation inductance L_m is 15 μH, the inductance values of the N_1 and N_2 windings are 15 μH and 154 μH, respectively, and the inductor L of the N_1 and N_2 windings in series is 265 μH.

In *Mode 4*, the energy of the leakage inductor L_k is transferred to C_C, and the capacitor voltage rises, so an appropriate capacitance value is required to prevent the capacitor voltage from being

too high. The voltage variation rate of u_{Cc} is set to be less than 10%. The voltage variation rate of u_{Cc} can be calculated using Eq. (17):

$$\Delta u_{Cc} = \frac{I_{Lm\max}}{C_C \omega_0} \leq u_{Cc}(t_4)10\% = \frac{N_1 u_{ab} + N_2 U_i}{10(N_1 + N_2)}, \tag{17}$$

where ω_0 can be expressed as Eq. (18):

$$\omega_0 = \omega = \sqrt{\frac{\left(\frac{N_1 + N_2}{N_2}\right)^2 + \frac{N_1^2 L_k}{N_2^2 L_m}}{L_k C_C}}. \tag{18}$$

Therefore, the calculated value of C_C is taken as Eq. (19):

$$C_C \geq \left(\frac{\sqrt{L_k} N_2 I_{Lm\max}}{0.1\,(N_1 u_{ab} + N_2 U_i)}\right)^2 = 27.9\,\text{uF}. \tag{19}$$

According to Eq. (19), the final value of $C_C$is chosen as 33 uF.

3.2. Design of ZVS operation

According to the analysis of high-frequency switch modes, in *Mode 4*, the inductor L_k charges C_C, causing an increase in the voltage across C_C. In *Mode 8*, the switch S_C is turned on and the current i_{Lk} drops rapidly. After S_C is turned off, i_{Lk} cannot change abruptly£¬and the parasitic capacitance voltage of the switch S drops rapidly to zero, providing the conditions for ZVS. The parasitic capacitances of switches S and S_C start to discharge at t_9 until the drain-source voltage u_{ds} of the switch S drops to zero in *Mode 10*. After t_{10}, the switch S is turned on to achieve ZVS.

The resonance process of *Mode 9* can be expressed by the following Eq. (20):

$$\begin{cases} U_i = L_k \dfrac{\mathrm{d}i_{Lk}}{\mathrm{d}t} + \dfrac{N_1 + N_2}{N_2} u_{ds} - \dfrac{N_1}{N_2} u_{ab} \\ i_{Lk} = i_{Lm} - \dfrac{N_2}{N_1} i_{N2} = 2C_{oss} \dfrac{\mathrm{d}u_{ds}}{\mathrm{d}t} + i_{N2} \end{cases}. \tag{20}$$

According to the above resonance analysis, the resonant period of *Mode 9* and the trans-zero time of the u_{ds} can be changed by changing the values of L_k and C_{oss}, and the latter also depends on the S_C conduction time T_{SC}. Therefore, the condition of achieving ZVS can be obtained as $u_{ds} \leq 0$.

Under this condition, a reasonable S_C conduction time and C_{oss}, both with respect to the inductor L_k, are shown in Eq. (21), and their curve with a different modulation factor K is shown in Fig. 8.

Therefore, the values of L_k and C_{oss} should be in the ZVS region of the above figure, where the minimum modulation $K_{\min} = 0.32$ occurs with the peak load.

$$L_k = \frac{\left(\frac{N_2 U_i + N_1 u_{ab}}{N_2}\right)^2}{\left(\frac{I_{Lm\max}^2 \cos(\omega_0 T_{Sc})^2}{C_C} + \frac{I_{Lm\max}^2 \sin(\omega_0 T_{Sc})^2}{2C_{oss}}\right)}. \tag{21}$$

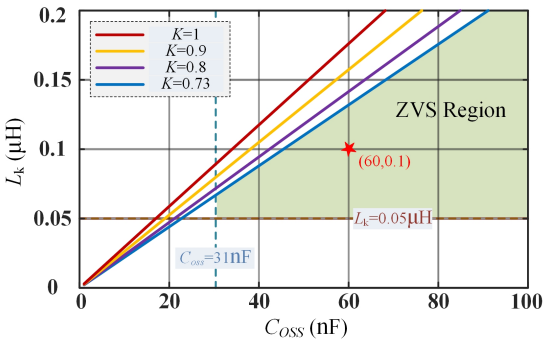


Fig. 8. Resonant parameters with different modulation K

In order to simultaneously reduce the MOSFET turn-off losses, ensure that the rising slope of the switch S drain-source voltage u_{ds} is small. The switch S parasitic capacitance should satisfy the following Eq. (22):

$$C_{oss} \geq \frac{I_{Lm\,\max} t_{\text{off}}}{\Delta u_{ds}}. \tag{22}$$

Through Eqs. (21) and (22), it is determined that the selected values for L_k and C_{oss} are 0.08 μH and 60 nF, respectively. In summary, the specific circuit parameter design can be obtained as shown in Table 2.

Table 2. Circuit parameters

Parameters	Symbol	Value
Input capacitor	C_{in}	2000 μF/35 V
Magnetizing inductor	L_m	15 μH
Leakage inductor	L_k	0.08 μH
Clamp capacitor	C_C	33 μF/250 V
Output filter capacitor	C_{filter}	6.6 μF/250 V
Load resistance	R_L	18 Ω
Parasitic capacitor	C_{oss}	60 nF/630 V

4. Experimental platform construction and validation

In this section, based on the circuit parameter design in Section 3, an experimental platform is built to verify the effectiveness of the studied CSI topology, three-stage SVPWM technique, and soft-switching for reducing switch losses. Due to the limitations of laboratory conditions, only resistive load experiments were conducted in the prototype testing. The prototype design parameters for the inductor windings are as follows: the rated output power is 1 kW, the rated input DC voltage $U_i = 24$ V, switching frequency $f_{sw} = 50$ kHz, and turn ratio $N_2/N_1 = 3$. The inductor

cores are made of the E-shaped core model S5530E from Dongmu Keda Corporation. The N_1 winding is made of 0.4×35 mm copper foil winding and the N_2 winding is made of 0.1×35 mm copper foil winding. The energy storage switch S and clamp switch S_C use IXYS IXFK230N20T and IXFH150N20T, respectively, S_1–S_6 use Infineon IGBT IKP15N60T, S_1–S_6 series diodes use Infineon diode IDDD12G65C6. The DSP control board uses the TI TMS320F28069 model. The DC power supply serves as the input power source for the driving circuit. The setup of the experimental prototype is shown in Fig. 9.

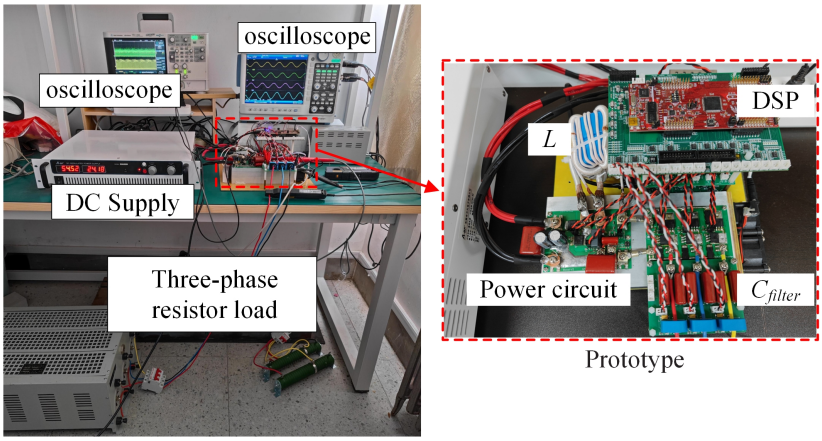


Fig. 9. Photograph of the experimental setup

Figure 10 shows the experimental waveforms of the CSI using three-stage SVPWM and soft switching. The experimental results indicate that:

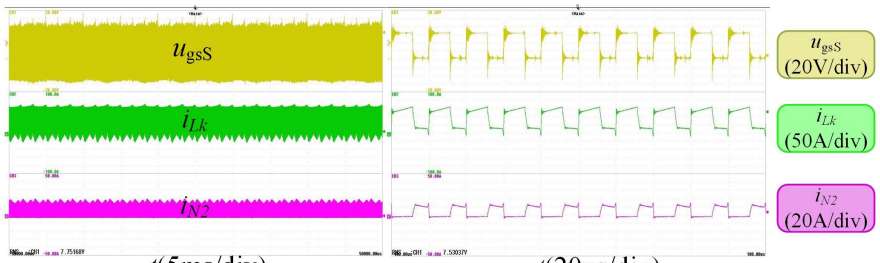
1. The energy storage inductor current and its high-frequency extension waveform are shown in Fig. 10(a). Before the switch S is turned off, the switch S_C is turned on and the current i_{Lk} drops rapidly, providing a renewal condition for the drop of the switch S drain-source voltage, which in turn achieves ZVS.
2. The waveform of the drive signal u_{gsS}, drain-source voltage u_{ds}, and their high-frequency extension waveforms of the switch S are shown in Fig. 10(b). After the switch S is turned off, a voltage spike appears in the drain-source voltage, but this voltage spike is limited by the clamping circuit. When u_{gsS} starts to cross zero, u_{ds} of the switch S has already dropped to zero, achieving zero voltage turn-on.
3. The waveform of the clamp circuit and its high-frequency extension waveform are shown in Fig. 10(c). After the switch S is turned off, u_{Cc} rises and remains constant. When the switch S_C opens, the voltage u_{ds} across the clamping capacitor decreases. When the switch S is turned on, the maximum voltage stress is the clamp capacitor voltage.
4. The DC-link voltage and its high-frequency extension waveform are shown in Fig. 10(d). As the inductor releases energy to the load, its voltage increases. The DC bus voltage responds to the AC side line voltage and demonstrates the three-stage modulation process.
5. The waveform of the drive signal u_{gsS1}, drain-source voltage u_{cS1} and series diode voltage of the switch S_1 on the a-phase bridge arm are shown in Fig. 10(e). When the switch is

turned off, the series diode bears the reverse voltage. The voltage to which the switching tube is subjected is the AC side line voltage.

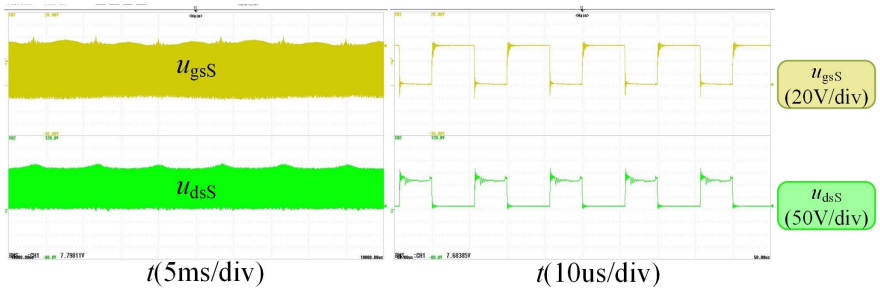
6. The output three-phase voltage and current waveforms are shown in Fig. 10(f). The experimental waveforms show that the output waveforms are of high quality and the prototype operates stably under three-stage SVPWM. The total harmonic distortion (THD) of the output current is 1.4%.
7. The soft-switching waveform is shown in Fig. 10(g). When the drive signal starts to cross zero, the drain-source voltage of the switch S has already dropped to zero, achieving zero-voltage turn-on.
8. The soft-switching waveforms for full load and light load cases are shown in Fig. 10(h) and Fig. 10(i), respectively. The soft-switching implementation reduces the voltage and current overlap region of the switch S, which significantly reduces the switching losses.
9. The dynamic response waveform of CSI output using three-stage SVPWM is shown in Fig. 10(j). It can be seen that the system is able to adapt to sudden changes in the actual operating environment.

Figure 11 shows the experimental prototype efficiency curves of the CSI with two different modulation techniques at various output power levels, where a rated power of 1 kW corresponds to 100% of the maximum power output.

When the output load power is higher than half of the load, the CSI conversion efficiency can be maintained above 95.4% using three-stage SVPWM. The circuit losses are mainly composed of switching conduction losses, inductor copper losses and inductor hysteresis losses. Due to the implementation of ZVS, switch losses are minimized.

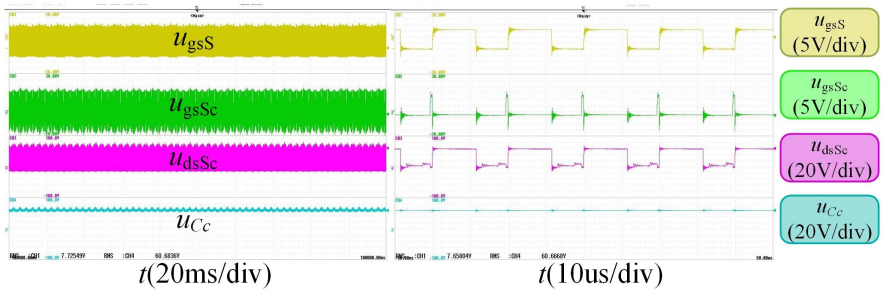


(a)

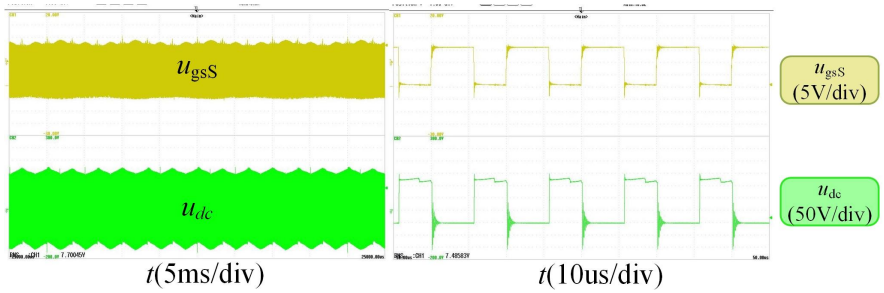


(b)

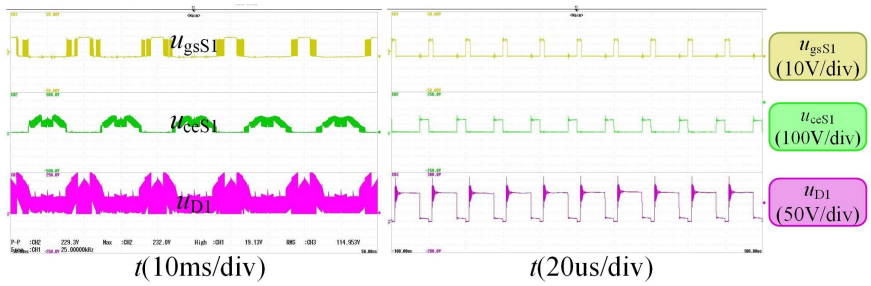
Fig. 10. [cont.]



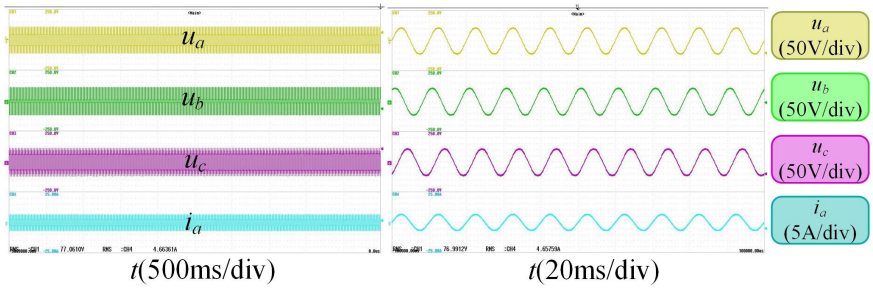
(c)



(d)



(e)



(f)

Fig. 10. [cont.]

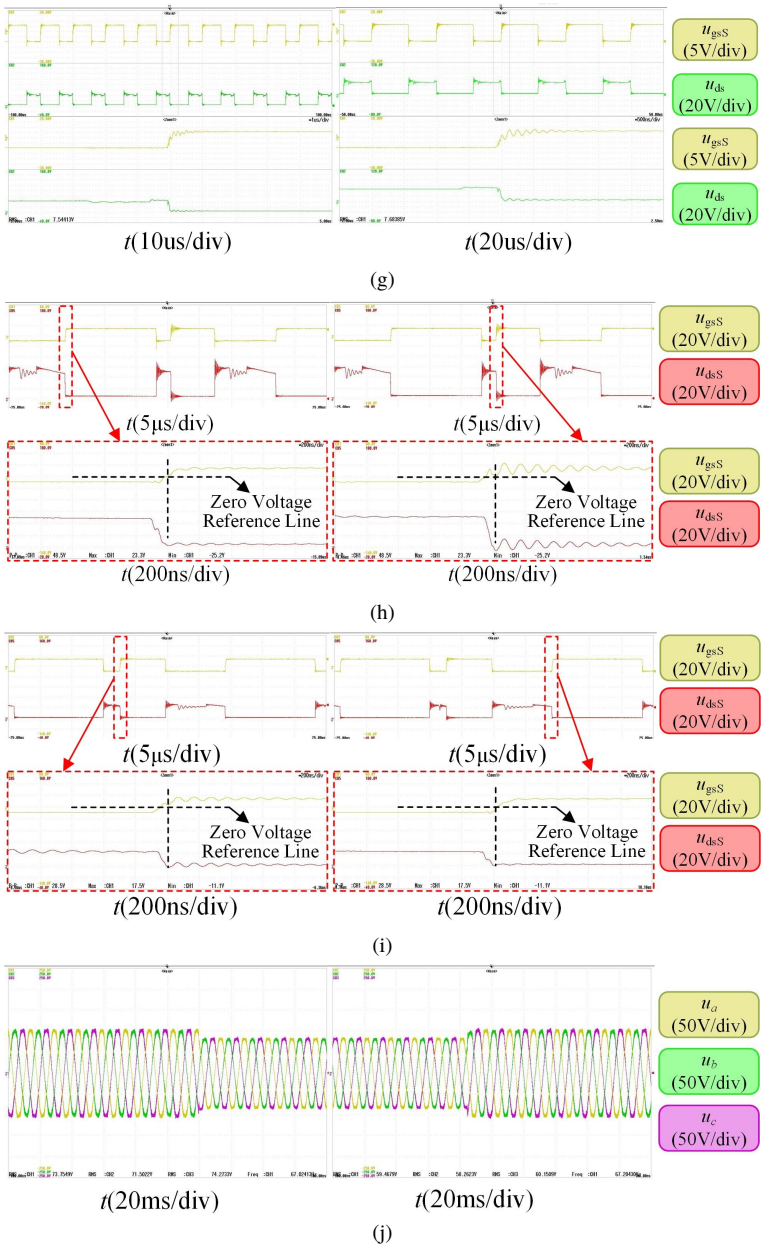


Fig. 10. Experimental waveforms: (a) energy storage inductor current i_{Lk} and i_{N2}; (b) the drive signal and drain-source voltage of S; (c) waveform of the clamp circuit; (d) the dc-link voltage; (e) drive signal u_{gsS1} and voltage stress of S_1; (f) the output three-phase voltage and current; (g) soft-switching implementation waveform; (h) the ZVS realization waveform in full load; (i) the ZVS realization waveform in light load; (j) dynamic response waveform

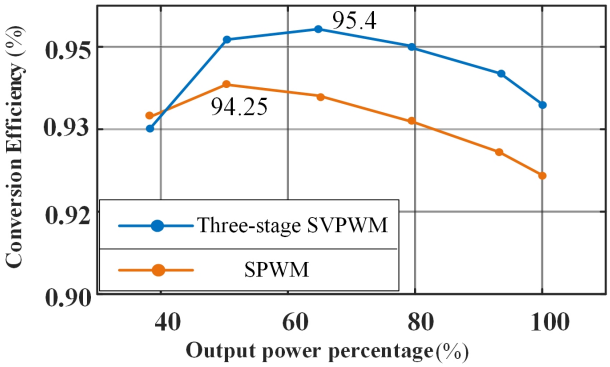


Fig. 11. Measured efficiency of the CSI

5. Conclusion

This article proposes a three-stage SVPWM strategy for the CSI with a large boost ratio, wide-range output, and high-power density. The main advantage of the proposed SVPWM strategy is that it achieves lower switching losses and improves the efficiency of the studied CSI compared to the conventional SPWM. The modulation is achieved by treating the on-state of the switch S as a zero vector and assigning effective vectors action modes. The ZVS of the switch S is achieved by the turn-on time of the switch S_C and the parameter design of the clamp branch. An experimental prototype is built to verify the modulation strategy, and it is found that compared to SPWM, the CSI peak efficiency is improved by 1.15% under full-load and half-load conditions.

Acknowledgements

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