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A TIME-DOMAIN PULSE AMPLITUDE AND WIDTH DISCRIMINATION METHOD FOR PHOTON COUNTING

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Abstract

This work shows a time-domain method for the discrimination and digitization of parameters of voltage pulses coming from optical detectors, taking into account the presence of electronic noise and afterpulsing. Our scheme is based on an FPGA-based time-to-digital converter as well as an adjustable-threshold comparator complemented with commercial elements. Here, the design, implementation and optimization of a multiphase TDC using delay lines shorter than a single clock period is also described. The performance of this signal processing system is discussed through the results from the statistical code density test, statistical distributions of measurements and information gathered from an optical detector. Unlike dual voltage threshold discriminators or constant-fraction discriminators, the proposed method uses amplitude and time information to define an adjustable discrimination window that enables the acquisition of spectra.

Keywords: Field-programmable gate array, time-to-digital converter, spectroscopy, photomultiplier, photon counting, discriminator, after-pulsing, low-voltage differential signalling.

1. Introduction

In Raman scattering and sometimes in fluorescence phenomena, very low level light intensity has to be detected by using *photomultiplier tubes* (PMT), *avalanche diodes* (APD) or *coupled charge devices* (CCD). With a PMT, its output current may be a train of analogue pulses or an analogue current generated by pulse piling. Typical output pulses from PMTs deployed for the intended application show typical amplitudes and widths that range from 10^{-12} A to 10^{-4} A and from 0.1 ns to 10 ns, respectively. In frequency-domain spectroscopy techniques, the earliest and most used method for pulse processing is a dual threshold discriminator and a digital counter [1]. Later on, alternative circuits were designed and implemented in order to process pulses with higher *signal-to-noise ratio* (SNR). For instance, refined discrimination and digitization systems for pulsed-response optical detectors take into account amplitude and width of pulses in order to determine some criteria to distinguish them from sources of perturbations such as cosmic rays, shot noise, residual ionization gases and any others generated by electromagnetic interference coming from any other equipment.

Among them, several methods have given a critical importance to front-end electronics, such as passive circuits in time-to-amplitude converters [2], constant-fraction discriminators [3] and

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alternative implementations of the phase-difference detection from lock-in amplifiers [4]. In contrast, in high-energy physics experiments, limitations in sampling speed and sensitivity of analogue-to-digital converters led to develop time-over-threshold discrimination [5] with refined pulse selection and measurement schemes for various pulse waveforms. In this method, the design and implementation of FPGA-based time-to-digital converters [6–9] fulfilled technical requirements of reading high numbers of optical detectors within a short dead time, on affordable, scalable, low power and miniaturized signal-processing equipment. Then, FPGA-based digitization was developed with TDCs and FPGA built-in LVDS buffers intentionally used as internal comparators [10]. Moreover, programmable logic now provides a fast sampling scheme that may also be refined towards a single-slope ADC with additional hardware [11–13].

Our aim was to develop an alternative to two schemes used in the photon-counting technique, constant voltage-threshold discrimination and constant-fraction discrimination, in order to alleviate common adverse situations in photomultipliers: fluctuation of voltage thresholds, background noise, pulse jitter and after-pulsing. This work shows a cost-sensitive readout system that offers an estimation of amplitude and time ranges of pulses from optical detectors, which will be used as criteria to distinguish them. This system is targeted for frequency-domain spectroscopy techniques and it is designed for its future use in time-domain spectroscopy techniques as well.

2. Time-interval measurement

Time-to-digital converters are used in experiments to determine sub-nanosecond time differences in applications such as position-emission tomography [8], high-energy physics experiments [6, 14], laser rangefinders [15] and time-resolved Raman and fluorescence spectrometers [16].

One of the hierarchical structures of fine time interpolation is the Nutt method [17], which was used here. It is a synchronization scheme for any measured digital signal that provides simultaneously high resolution and high dynamic range. This method generates a coarse signal in function of the clock reference signal and two fine signals (called start and stop signals, respectively) that last less than an entire clock period (Fig. 1). The fine start signal (ΔT_1) is the time difference between the rising edges of the measured signal (also regarded as meas. signal), and the clock reference signal within a period, whereas the fine stop signal (ΔT_2) is the time difference taken from their respective falling edges. The coarse signal (ΔT_{12}) represents the clock cycles the measured signal completes. Hence, the measured time T_x is depicted in (1). Delay lines interpolate fine signals, and digital counters interpolate the coarse signal.

$$T_x = \Delta T_1 + \Delta T_{12} - \Delta T_2 \tag{1}$$

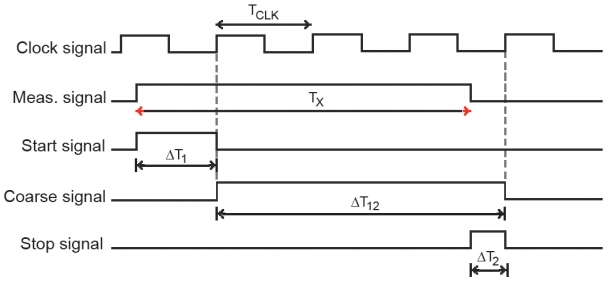

Fig. 1. Waveforms generated by the Nutt method.

3. Discrimination and digitizing scheme setup

The system for acquisition of spectra consists of two components: one optical and one electronic. In the optical component, elements are arranged for the analysis of a mercury lamp; these being a diaphragm, a lens and the lamp itself. The recollected light goes to an Oriel Cornerstone 130 monochromator, in which one of the two diffraction gratings is selected and rotated around any wavelength of interest between 100 nm and 1000 nm. The filtered light goes to the Hamamatsu R2295 PMT, which is powered by a high-voltage divider circuit. From there, the electronic component takes place in order to process the PMT output current pulses. Its signal is conditioned by a Mini-circuits ZX60-P103LN+ module, based on a broadband and low electronic noise trans-impedance amplifier. The resulting signal is compared to a constant voltage threshold adjusted by a MAX5825 digital-to-analogue converter.

A time and amplitude discriminator was developed within the Xilinx Spartan-6 XC6SLX45T FPGA on a Xilinx SP-605 board. An LVDS buffer is intentionally used for this operation. During the time the signal has a higher level than the threshold, a digital pulse is created and the TDC measures its width. Once its output codes are released, there are two paths to process them. The first, taking them to an event counter, which compares the time result between two time thresholds, giving valid counts per second during the acquisition of spectra. This path is controlled by a Java application and the Microblaze processor. Beyond that, the other path stores a large amount of TDC samples in an external 128 MB RAM memory. Later, it transfers them to the computer via an USB-UART interface, for the purpose of TDC characterization and estimation of pulse parameters, such as amplitude, duration and repetition rate. This stage is supported by executable files that arrange all data and compute any figure of interest.

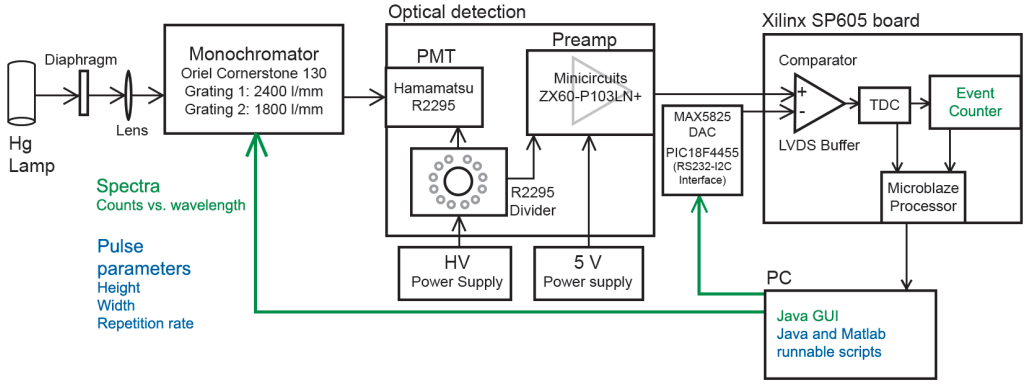

Fig. 2. The system setup.

4. Design and implementation of TDC

The TDC contains four interpolators, each one taking a PLL phase as their clock reference. Each interpolator consists of two fine synchronizers, one for the start and another for the stop signal, a coarse synchronizer, a coarse counter, and two delay lines with their own pre-encoder. The results given by each interpolation phase are preprocessed in a finite state machine.

Even though the chosen FPGA has high-speed capabilities and some modules of high-end families such as Xilinx Virtex 5 and 6, it has one of the smallest areas to work with. Using delay

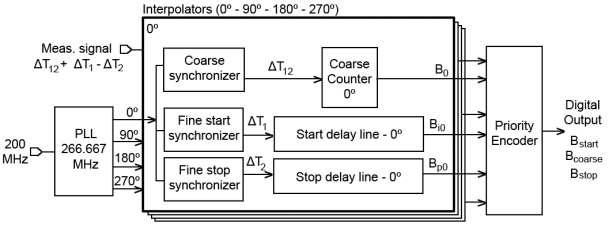

Fig. 3. The TDC architecture.

lines that cover the entire clock period were avoided due to clock region crossings [8], which increase non-linearity and skew. Therefore, the proposed architecture uses four shorter delay lines that cover the entire clock period. We also used strict and extensive timing and placement constraints, and manually placed logic primitives belonging to delay lines and synchronizers. No manual routing was done in order to facilitate a migration to other FPGA families.

4.1. Synchronizers for TDC

Other authors have designed and implemented TDCs with multiple phases before [18-20]. Here, four delay lines cover the entire clock period, and the clock period exceeds the length of the delay line. Then, the design and implementation of synchronizers for the Spartan-6 family is shown for this particular case from a timing closure perspective [21], along with additional considerations for the calibration method in the characterization of the TDC [22].

An expression to find the maximum operating for flip-flops also gives the maximum delay that both combinatorial logic and routing added can reach (T_{Net}), from $(T_{CLK}, 3750$ ps) calculated from the PLL frequency. Skew $(T_{Skew}, 95$ ps), clock-to-output $(T_{CKO}, 450$ ps) and setup $(T_{SU}, 420$ ps) times are given parameters by [23]:

$$T_{CLK} > T_{CKO} + T_{SU} + T_{Net} + T_{Skew}. \tag{2}$$

The net delay (2785 ps) introduced within the synchronizers might easily exceed the maximum found using (2). Emulating the effect of transferring a bit within a quarter clock period and avoiding ambiguities is mandatory [18]. This was done by means of a chain of an even number of inverters, equivalent to a delay line of the entire clock period.

Fine and coarse signals were generated in separate synchronizers. In the fine synchronizer shown in Fig. 4 (left), start (ΔT_1) and stop (ΔT_2) signals are generated. The rising edge is generated by the measured signal whereas the clock signals generate the falling edges. FF1 is used

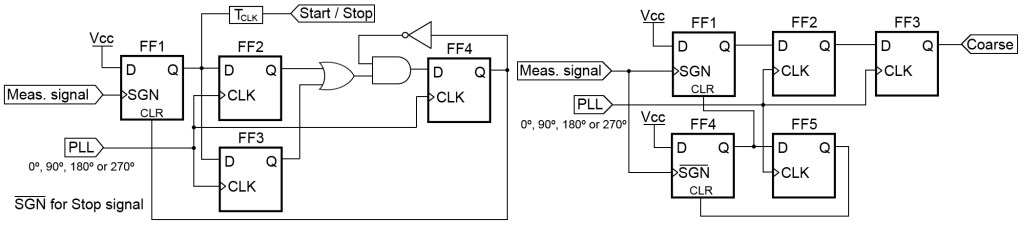

Fig. 4. Synchronizers for (left) fine and (right) coarse signals.

to detect the rising edge and its output is sampled by both FF2 and FF3 in order to reduce meta-stability failure rate. After a clock period, FF4 clears FF1. Also, FF1 output was followed by the mentioned chain of inverters. However, synchronizers do not make a perfect cut of fine signals due to PVT fluctuations, PLL signal jitter and flip-flop meta-stability. Then, the begin taps and end taps of each delay line must be determined by the results given by the statistical code density test. Meanwhile, the coarse signal (ΔT_{12}) is generated by the synchronizer shown in Fig. 4 (right). Two clock periods after detecting the rising edge of the signal and once its falling edge is detected, FF1, FF4 and FF5 are cleared. This coarse synchronizer has a dual-edge detection feature, so signals are detected even if the clock is in its low level.

4.2. Time interpolation and encoding

Given the mentioned consideration for net delays, fine signals are measured in a fine delay of 16 cascaded CARRY4 primitives, equivalent to 64 taps. CARRY4 primitives were chosen because they require less area, generate lower interpolation times [24] and are easier to calibrate. Their length is about slightly longer than a quarter period (1280 ps), thus enabling the capability of measuring the begin taps and end taps of all delay lines. The results from the delay lines are extrapolated by a stepped-up encoder designed by [25] and adapted for simple tapped delay lines.

Coarse signals are measured with digital counters. Coarse counters are divided in two types in order to keep low dead time and high dynamic range. Then, four Johnson counters and one Gray counter are used to measure time intervals up to 200 ns and 9 µs, respectively. Additional coding and processing is performed by a finite state machine. The coding task is split in six clock cycles: three of them are used to extrapolate the results of all delay lines, two to process the results of all coarse counters, and the last one to generate a 64-bit word.

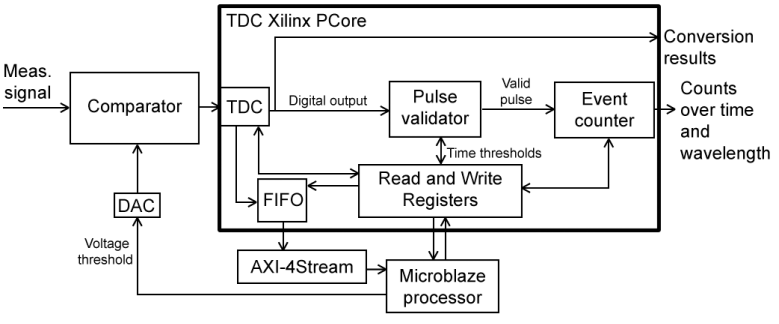

Fig. 5. The developed digital architecture.

Next, the 64-bit result goes to a FIFO-memory, which transmits data to the RAM memory through AXI-4 DMA core in the burst mode. The stream is retrieved by the Microblaze processor and then transmitted to the PC via the USB-UART interface. This digital architecture was developed by creating a Xilinx *PCore*. The primitives belonging to this core were placed and routed implemented in the south region. Many primitives were automatically placed and routed, except for the measurement and encoding blocks. The blocks belonging to delay lines were located in clock regions X0Y1-X1Y1. Also, most primitives from these blocks were placed manually. The blocks belonging to coarse counters and the priority encoder were placed in clock regions X0Y2-X1Y2. These clock regions were chosen by their number of SLICEM blocks available.

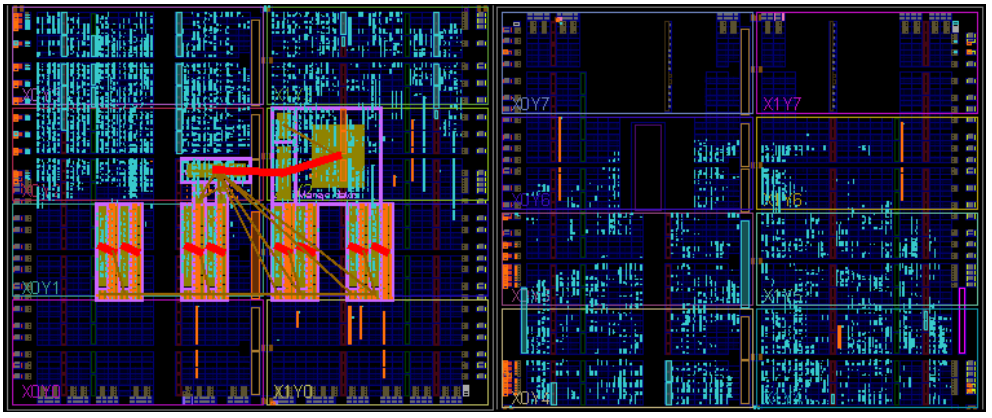

Fig. 6. FPGA fabric. (Left) South region. (Right) North region.

4.3. Statistical density code test

Delay line readout ambiguity is displayed as several nonzero values among either start and or stop lines. This leads to contradictory results after applying (1).

Table 1. Samples with ambiguous results.

COARSE COUNTS	TAPS REACHED IN STOP LINES				TAPS REACHED IN START LINES			
	270º	**180º**	**90º**	**0º**	**270º**	**180º**	**90º**	**0º**
5	26	2	0	0	0	28	0	0
6	0	0	34	2	2	2	0	46
5	48	7	0	0	0	0	22	0
5	1	0	0	28	47	2	0	0

Let 1, 2 and 3 be three adjacent delay lines. They all have a 90° phase difference. After having all results of the statistical code density test, the begin tap and the end tap of delay line 2 can be found. The begin tap A can be found from the zero elements of lines 1 and 3, looking for the minimum tap value for delay line 2. The stop tap B also can be found from the zero elements of lines 1 and 3, looking for the maximum tap value for delay line 2. Then, the C values of delay line 2 are replaced as follows:

$$C' = \begin{cases} 0 & \text{if } C \leq A \text{ or } C > B \\ C - A & \text{otherwise} \end{cases} \tag{3}$$

For instance, the results of the 180º start line will be corrected. The found values for A and B are 8 and 51. This means that the effective delay line length $(B-A)$ is 44 taps. Also, the values 28 and 2 change to 10 and 0, respectively.

After computing the lengths of all delay lines and correcting all values, the actual measurement range (MR_j) of a j delay line can be determined as:

$$MR_j = \frac{TN_j}{N}, \tag{4}$$

where T is a clock signal period; N is the total number of samples taken and N_j is the number of samples corresponding to delay line j. The value of time step per tap is given by the measurement range of each delay line, multiplied by the number of samples in tap i, C_i; and divided by the accumulated samples up to tap i, $\sum_{1}^{i} C_i$:

$$T_{tap} = \frac{MR_j C_i}{\sum_{1}^{i} C_i}. \tag{5}$$

Then, an average resolution per delay line can be found:

$$T_{LSB} = \frac{MR_j}{B-A}. \tag{6}$$

Each time step is found as:

$$t_i = \frac{C_i MR_j}{N_j}. \tag{7}$$

The differential *non-linearity* (DNL) in a tap i describes the deviation of each time step from its average value T_{LSB}, and *integral non-linearity* (INL) is defined as the sum of DNL accumulated up to a tap i:

$$DNL_i = \frac{t_i - T_{LSB}}{T_{LSB}}. \tag{8}$$

$$INL_i = \sum_{i=1}^{i} DNL_i. \tag{9}$$

5. TDC non-linearity and uncertainty of measurements

An external 27-MHz crystal oscillator introduced in a clock socket, an FPGA built-in frequency synthesizer and the very PMT current were used as test signals, each one separately. The measurement data were transmitted to the PC through the USB-UART interface running at 115200 baud/s.

Obtained with the statistical code density test, the nonlinearity is plotted in the following figure. 128×10^3 samples of the 27-MHz crystal oscillator were collected. The performed test indicates that DNL varies between -1 LSB and 2.93 LSB, and INL varies between -2.79 LSB and 3.15 LSB.

The actual distribution of time through taps from delay lines is shown:

Table 2. Attributes of delay lines.

START LINES	B – A	MR (ps)	T_{LSB} (ps)	STOP LINES	B – A	MR (ps)	T_{LSB} (ps)
0°	47	923	19.65	0°	48	972	20.69
90°	44	937	21.3	90°	40	895	22.38
180°	41	889	21.68	180°	36	821	22.82
270°	48	999	20.82	270°	45	1060	23.55

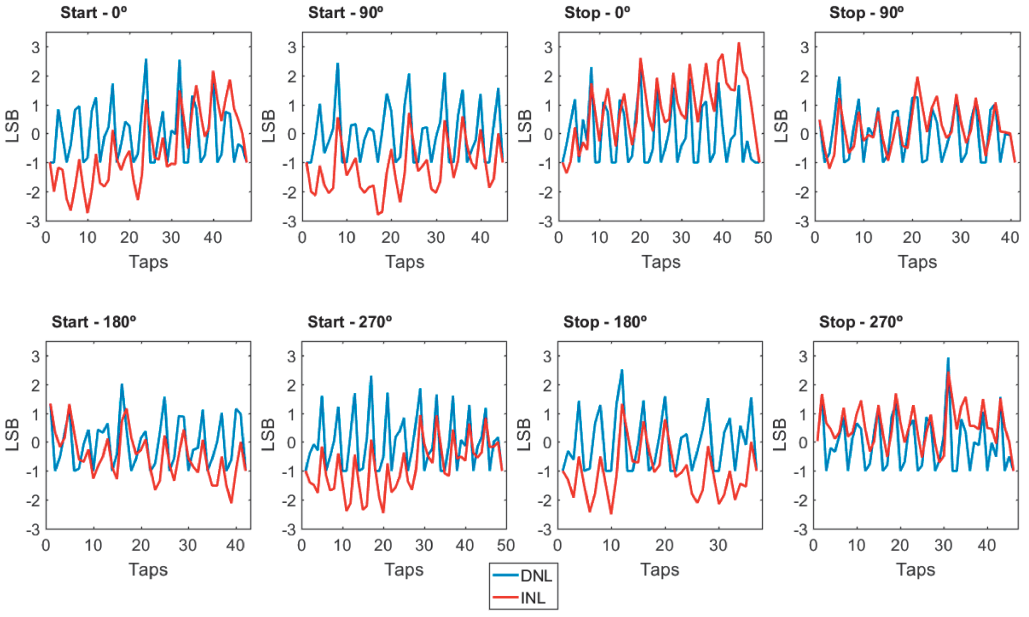

Fig. 7. DNL and INL of all delay lines.

The duration of the high voltage level of the 27-MHz crystal oscillator signal was measured. Its average and standard deviation were found, and its time distribution is displayed in Fig. 8. The smaller peaks take place at ±3750 ps from the main peak. Their source is the remaining meta-stability failure rate in flip-flops belonging to coarse counters. The main result is displayed next to another peak. The distance between them is 937 ps, which is the time difference between the phases used for interpolators. Its source may be the generation of longer or shorter fine signals due to meta-stability in flip-flops belonging to synchronizers. Results associated with this peak report higher tap values of stop lines whereas there are null results for start lines that compensate them.

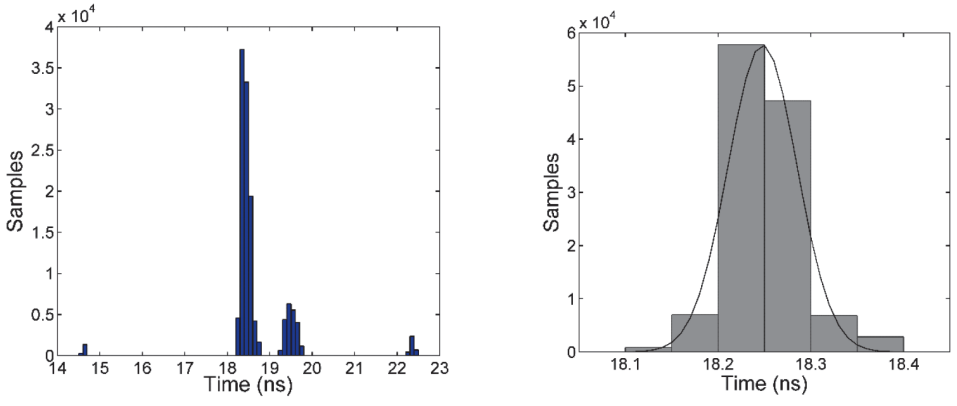

Fig. 8. Results before and after correction.

The shifted peaks were corrected through probability-based clustering by means of an algorithm based on functions for Gaussian mixture models [26]. First, a known number of peaks (as clusters) and an initial set of values for the average and standard deviation for each peak are given. Then, a number of interactions is set. For every sample, the probability of belonging to a peak is found, and it is associated with the peak with the highest value. Through interactions, the association of samples with peaks is optimized. At the end, the algorithm reports the average and standard deviation of all optimized peaks. Finally, the shifted peaks are merged with the main one, which corresponds to the main result of measurements.

The 27-MHz crystal oscillator signal was also modified with a DCM (FPGA digital clock manager) in the dynamic reconfiguration mode [27], which acts as an internal frequency synthesizer. In addition, a Tektronix AFG3021B signal generator was used to measure several time intervals as well. Table 2 shows peak information for all plots. In general, signals from DCM variations show more jitter than signals from the external generator. Then, a DCM generates additional electronic noise that makes peaks broader and less defined.

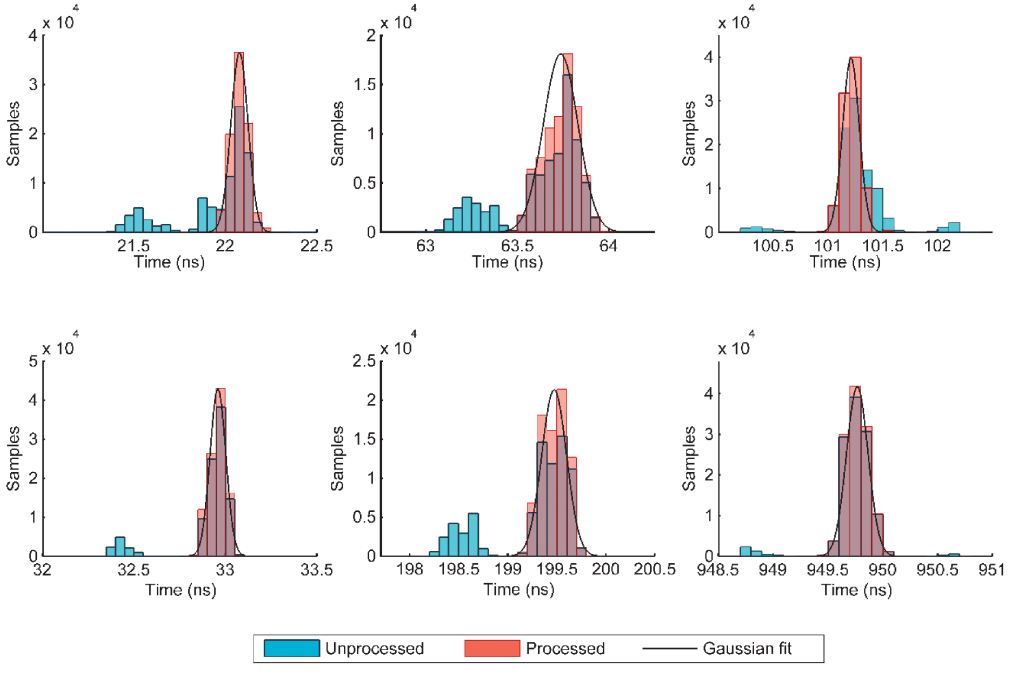

Fig. 9. Time spectra acquired for DCM variations (top plots). Time spectra acquired for intervals adjusted with the external signal generator (bottom plots).

All plots demonstrate that the generation of falling edges in fine synchronizers using a crystal oscillator has a disadvantage. The crystal oscillator in conjunction with a PLL generates an important amount of jitter that affects the generation of fine signals, either stretching the pulses near the begin and end taps of a delay line or shrinking them so they cannot be measured at all. However, the Gaussian mixture algorithm proves to be a valuable tool for the estimation of parameters of all peaks, and to merge results within a single peak. Also, it helps refine results by calculating a more accurate average and a lower standard deviation.

Table 3. Attributes of peaks found before and after correction.

	UNCORRECTED		CORRECTED	
	μ (ns)	σ (ns)	μ (ns)	σ (ns)
DCM 1:1 (Multiply:Divide) Ratio – 18518 ps				
Peak 1	18.47	0.09	18.50	0.08
Peak 2	19.50	0.12		
DCM 5:4 Ratio				
Peak 1	22.95	0.42	23.16	0.09
Peak 2	23.09	0.16		
DCM 2:7 Ratio				
Peak 1	63.52	0.17	64.47	0.19
Peak 2	64.47	0.19		
DCM 2:11 Ratio				
Peak 1	100.38	0.13	101.21	0.07
Peak 2	101.26	0.12		
Peak 3	102.11	0.06		
Signal generator – 34 ns				
Peak 1	32.87	0.09	33.92	0.09
Peak 2	33.92	0.09		
Signal generator – 200 ns				
Peak 1	199.03	0.12	199.97	0.13
Peak 2	199.97	0.13		
Signal generator – 950 ns				
Peak 1	948.80	0.08	949.77	0.09
Peak 2	949.77	0.10		
Peak 3	950.63	0.07		

6. Discrimination of photomultiplier signal

The pre-amplified PMT signal under low light levels shown in Fig. 10. It was captured with a Tektronix TDS2014B oscilloscope in the persistence mode. It exhibits after-pulsing. Nonetheless, it should be pointed out that the first pulse has a great amplitude jitter, which is consistent with a typical PMT waveform. Also, the results from the digitization system are compared with the pulse shape.

In the acquisition of the time spectra from the PMT signal, lower voltage thresholds (up to 400 mV) report similar curves, indicating that the pulses from the PMT are being picked up along with after-pulsing and other sources of noise. However, this does not happen for a 500 mV threshold, in which the shape is scaled, indicating the presence of more counts due to light. For a 600 mV threshold, the shape is distorted. This is due to the shortening of time intervals generated by the comparator under higher thresholds. For all plots, the PMT signal takes time intervals between 2 and 7 ns, which is consistent with pulse widths. These are the time limits that will be considered by the event counter.

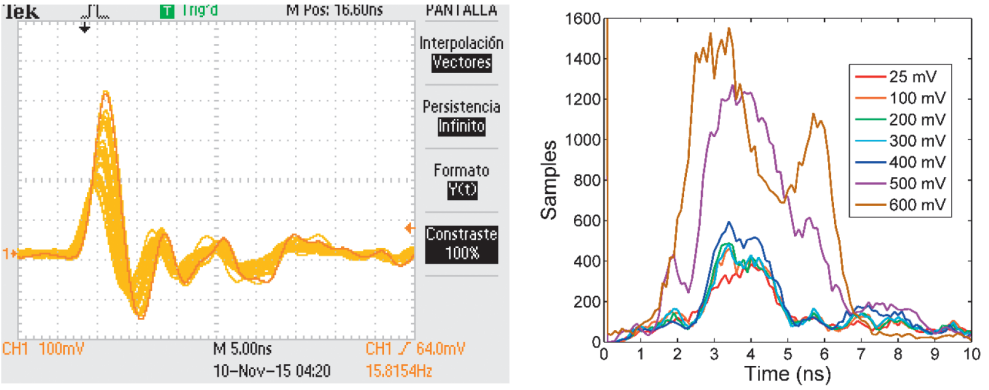

Fig. 10. Examples of actual PMT output pulse waveforms (left). Time distribution of pulses under voltage thresholds for the PMT (right).

6.1. Acquisition of light spectra

Several pulse height distributions were taken under three different light levels from a mercury lamp. For middle and higher light levels, count rates are higher and curves are broader. From 500 mV and up, the registered counts are proportional to light levels. Therefore, the entire system is able to distinguish the PMT signal in the presence of noise.

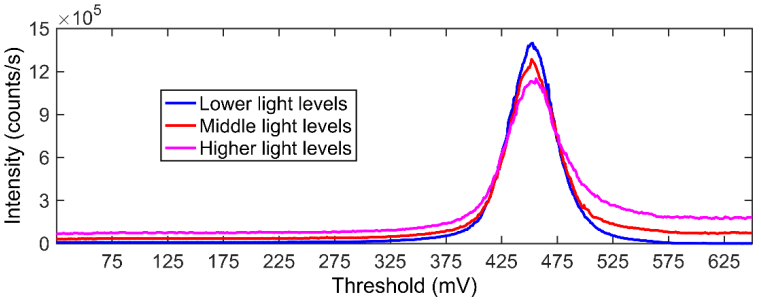

Fig. 11. Pulse height distributions of PMT pulses under a 2–7 ns time interval.

Both time information from Fig. 8 (right) and amplitude information from Fig. 9 confirm that the signal is present in higher voltage thresholds, from 500 mV and up.

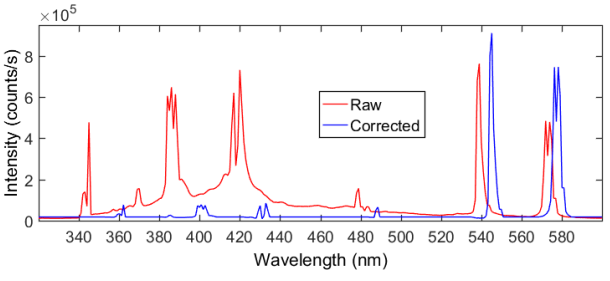

Fig. 12. A spectrum acquired from a mercury lamp.

The acquisition of spectra was configured with a 2–7 ns time interval and a 600-mV voltage threshold. The Hamamatsu R2295 PMT was fed with 1000 V and a 10-μm slit was used at the input of the monochromator. The raw emission spectrum was corrected by wavelength, relative intensity, noise suppression and background elimination with methods proposed by S.J. Baek, *et al*. [28].

7. Conclusions and outlook

The developed discrimination and digitization scheme can detect differences between pulses and noise. This means that it can work in the conditions of poor analogue signal processing. Also, it is capable of detecting differences in levels of light. In conjunction with a TDC and a DAC, the range of pulse height and width of pulses for both optical detectors were found and successfully compared with data obtained from an oscilloscope. These data were used to define discrimination parameters in the acquisition of spectra. Then, this work uses both time and amplitude information to set optimum discrimination parameters, unlike commercial spectrometers or signal discrimination modules. Furthermore, this means the scheme itself may be used to identify a discrimination window without the aid of testing equipment, such as oscilloscopes.

For the developed multiphase TDC, we proposed a method to correct delay line readout ambiguities. However, this method needed support of a Gaussian mixture algorithm, due to the need of clustering results and reporting only one average and standard deviation of measurements. For future works, we consider the generation of fine signals in synchronizers as a topic of improvement for measurement of signals that last less than a single clock period.

This system will be further refined and used with an optical detector capable of detecting Raman scattering, in order to acquire spectra of low cross-section samples in powder. In particular, we intend to obtain spectra of samples of carbon nanostructures and iron oxides in the short term.

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