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Analytical and experimental determination of the parasitic parameters in high-frequency inductor

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Abstract. The paper presents the results of calculations, simulations, and measurements of parasitic capacitance of winding in ferrite inductor suitable for cooperating with 2 kW DC-DC boost converter built using SiC JFET transistors, operating with a switching frequency of 100 kHz. The inductor winding is made of litz wire in a two-layer configuration. The lumped model of inductor winding was adopted. The results of analytical calculations have been compared with the results obtained from experimental investigations based on the resonance effect.

Key words: model of inductor circuit, interlayer capacitance, parallel resonance, litz wire, inductor winding, skin effect.

1. Introduction

Nowadays, new wide bandgap (WBG) power semiconductor devices made from silicon carbide (SiC) or gallium nitride (GaN) are increasingly being used in power electronics converters [1–6]. Magnetic components, like transformers or inductors, are also indispensable parts of many power electronics converters [7–10]. Fast switching transients, characterized by tens of nanoseconds for turn-on and -off processes and related high-voltage applications of SiC devices, can contribute to occurring of some undesirable parasitic phenomena. High values of dv/dt appearing in these devices trigger new problems, which have not yet been observed in circuits with silicon (Si) semiconductors. The main cause of these problems is related to parasitic capacitances, mainly output capacitances of transistors and diodes, and also capacitances of windings in magnetic components [11–14]. As has been shown in previous works [13], these phenomena have a significant role in the correct operation of converters. High values of parasitic capacitance of inductor winding can have a negative impact and cause additional switching power losses and EMI problems [15]. Estimation of capacitance values in magnetic components is becoming an important issue in the design process, next to the determination of basic parameters like inductance, number of turns, or saturation current [16].

This paper is focused on the determination of global parasitic capacitance of an inductor with inductance equal to $L = 1.2$ mH and dedicated for cooperating with nominal power $P_n = 2$ kW DC-DC boost converter, built with SiC devices, operating with switching frequency $f_s = 100$ kHz. Special attention is paid to analytical description and presentation of the experimental measurement method, which uses damped resonance. Results from both parts – analytical calculations and experimental investigation – have been compared.

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2. Model of high-frequency inductor

The most common method for determining typical parameters of an inductor in a converter design process is the equivalent circuit method, which takes into account the lumped parameters of this component (Fig. 1). Essentially, the parasitic capacitance is treated as the capacitor C_p, connected in parallel to the inductor. This capacitance is connected in parallel to the resistance R_p, which corresponds with the power losses in the core. Also, both C_p and R_p are connected in parallel to the third leg, consisting of a series connection of inductance L and resistance R_s, representing the total resistance of the winding.

A laboratory model of the inductor has been build using a UI93 core made from N87 type ferrite, which is characterized by the effective cross section area $S_{Fe} = 840$ mm^2 and volume $V_{Fe} = 220$ cm^3, as provided in the core's datasheet. Knowing these parameters, in order to achieve the assumed inductance $L = 1.2$ mH at nominal current $I_{max} = 8$ A, the winding with the number of turns $N = 40$ has been prepared. In order to reduce the eddy currents and winding losses in the assumed frequency of 100 kHz, a litz wire, made up of 120 wires of 0.1 mm di-

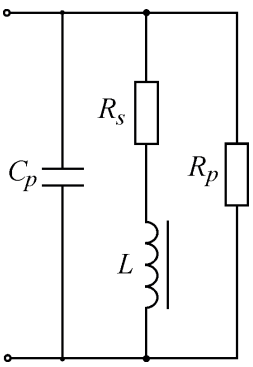

Fig. 1. Equivalent circuit of a high-frequency inductor with lumped parameters

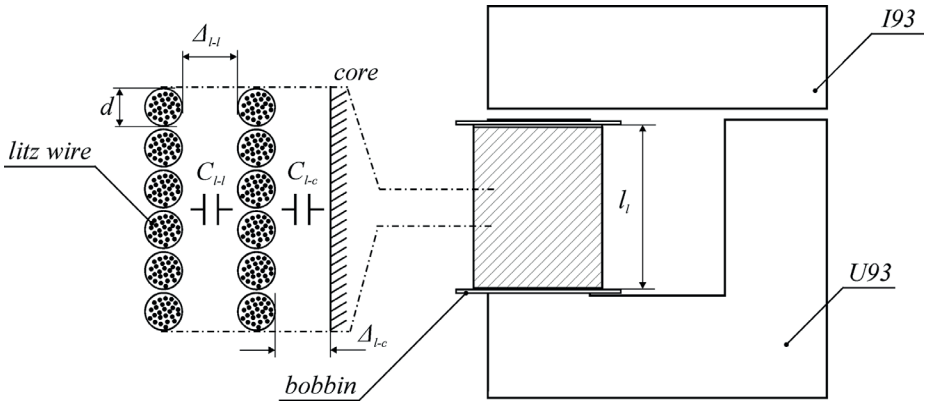

Fig. 2. Layout of high-frequency inductor with ferrite core and double-layer winding

ameter each, has been used. A two-layer coil with 20 turns per layer was made, where the first turn of the top (outside) layer was placed on the last turn of the bottom (inside) layer. The width of each layer was $l_l = 4.5$ cm (Fig. 2), and the distances between the bottom layer and the core (Δ_{l-c}) and between layers (Δ_{l-l}) have been set to 0.2 mm with the use of Kapton tape.

3. Analytical calculations

Analytical determination of inductor parameters can be performed only when all the information about the construction and realization process is well known. Such information, like the type of material, shape and geometrical dimensions of the core should be known. The construction of the winding and the electrical properties of wire material are also required. One of the methods for analytical determination of parasitic capacitance of the winding assumes that the layers of the winding are treated as capacitor plates. In the case of two-layer winding, the total parasitic capacitance C_p of the inductor winding can be calculated from [17, 18]:

$$C_p \cong \frac{C_{l-c}}{12} + \frac{C_{l-l}}{3}, \tag{1}$$

where C_{l-c} represents the capacitance between the bottom layer and the core, and C_{l-l} is the interlayer capacitance.

For multilayer winding, capacitance between the first layer and the core (C_{l-c}), being a minor part of total capacitance of winding, can be neglected [13, 15]. In this case, interlayer capacitance C_{l-l}, which is a dominant part of the total parasitic capacitance of the two-layer winding, can be described using:

$$C_{l-l} = \varepsilon_0 \varepsilon_r \frac{S}{l_{l-l}} = \varepsilon_0 \varepsilon_r \frac{l_N l_l}{l_{l-l}}, \tag{2}$$

where l_{l-l} is the thickness of distance between the layers (the dielectric area), S is the surface area of the capacitor plate and is equal to the area of the layer, ε_0 equal $8.854 \cdot 10^{-12}$ F/m is the dielectric constant of vacuum, ε_r is the relative dielectric constant of the distance between the layers, and l_N and l_l are the average length of turn and width of the layer, respectively.

The thickness of distance l_{l-l} can be calculated using the following equation [18]:

$$l_{l-l} = \Delta_{l-l} + 1.26 d_0 - 1.15 d, \tag{3}$$

where Δ_{l-l} is the thickness of distance between inner parts of layers (Fig. 2).

The averaged diameter of the litz wire d_0 and the averaged diameter of the effective cross-section of copper d can be expressed by:

$$d_0 = d_L \sqrt{\frac{4N_s}{\pi}} \tag{4}$$

and

$$d = d_L \sqrt{N_s}, \tag{5}$$

where: d_L is the diameter of a single strand, and N_s is the number of wires in the litz wire.

The parasitic capacitance of windings for the presented inductor layout has been calculated using equations (1–5), from which a value of $C_{p(a)} = 157.5$ pF was obtained.

The resistance of winding, determined for DC current ($R_{s\text{-}dc}$), has been calculated based on the length of the wire ($l_{Cu} = 7.2$ m), the effective cross section of the wire ($S_{Cu} = 0.94$ mm^2), and resistivity of copper ($\rho = 1.72 \cdot 10^{-8}$ Ωm) in a temperature of $T = 20$°C. The result of this calculation was $R_{s\text{-}dc} = 100$ mΩ. Resistance for AC current $R_{s\text{-}ac}$ has a similar value to the resistance for DC current, due to the fact that the diameter of a single strand of the used litz wire has a value smaller than the penetration (skin) depth, equal $\delta = 0.21$ mm, calculated for a frequency $f = 100$ kHz and a temperature of 20°C. As shown in the next parts of the paper, the resonant frequency, resulting

from the circuit parameters (Fig. 1), is about 360 kHz. For that value, the penetration depth equals $\delta = 0.11$ mm, so for that case we can also assume that $R_{s\text{-}ac} = R_{s\text{-}dc}$.

Parallel resistance R_p can be calculated from

$$R_p = \frac{U^2}{P_{Fe}}, \tag{6}$$

where P_{Fe} is core power losses and U is the voltage at the inductor.

The resistance R_p is a nonlinear function of induction in the core. In laboratory conditions, presented in the next section, when voltage across the inductor is equal to 10 V, the calculated parallel resistance R_p is close to 60 kΩ.

4. Measurements

The measurement method is based on parallel resonance, and it uses single-pulse excitation. The inductor current is interrupted by a transistor switch (Fig. 3a) resulting in self-damped oscillation. For this experiment, fast SiC JFETs (junction-field-effect-transistor), SJDP120R085 type transistors have been used. To accurately determine the parasitic capacitance of the inductor winding, besides the parameters of the inductor depicted in Fig. 1, that is R_s, L, C_p, and R_p, it is necessary to take into account the parameters of switch (C_T) and voltage probe of scope (C_{sc}). The resistance of conducting transistor $R_{T(on)}$, the internal resistance of voltage source R_E, and the resistances of connections are neglected and equated to zero. It was also assumed that the resistance of the non-conducting transistor is tending to infinity. Because the output capacitance of switch has a nonlinear characteristic and this capacitance depends on V_{DS}, the presented method requires at least two measurements – one with a single switch, and another one with two switches set in parallel (Fig. 3c). If the two switches are identical, it can be assumed that they have the same parasitic capacitance (C_T), which was added to the parasitic capacitance of the inductor (C_p). In addition, the capacitance of the voltage probe (C_{sc}) should be considered.

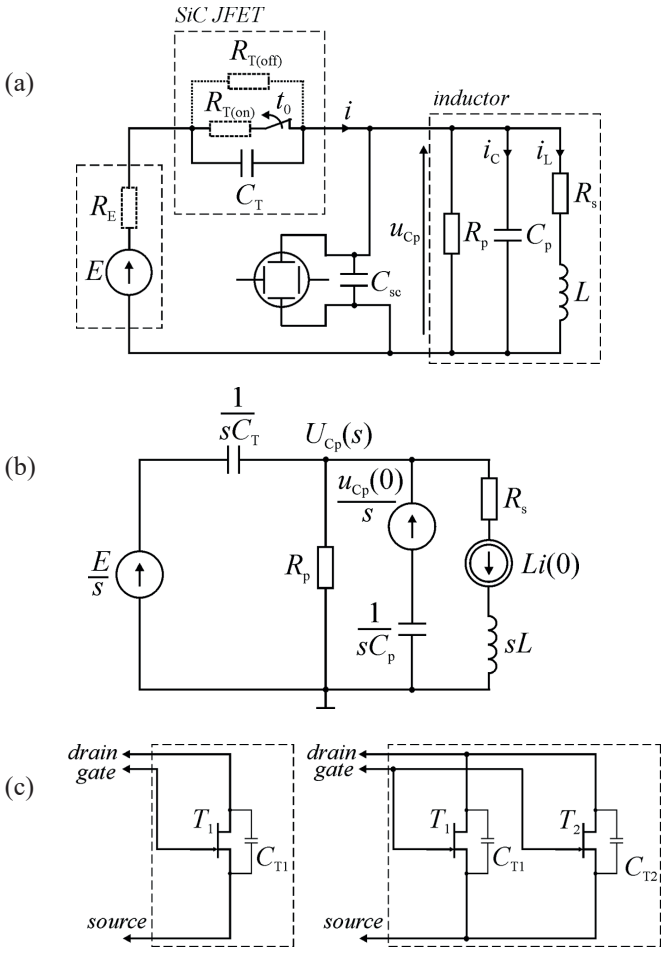

Fig. 3. Circuit scheme for determining parasitic capacitance of inductor using parallel resonance method (a), scheme in s domain (b) and scheme of switch configuration (c)

To better explain the presented measurement method, the circuit depicted in Fig. 3a can be represented by a schematic in domain s (Fig. 3b). Using the nodal method, the equation for node $U_{Cp}(s)$ can be expressed with (7). The analysis of the initial conditions indicates that at time t_0, when the transistor is switched off, the voltage across the capacitor C_p and the current in the leg with inductance L are $U_{Cp}(0) = E$ and $i(0) = E/R_s$ respectively. Taking these conditions into account, after the transformation of equation (7), the equation (8) has been obtained. The solution to the characteristic equation, which is the denominator in the equation (8), is a pair of characteristic roots (9).

$$\left(sC_T + \frac{1}{R_p} + sC_p + \frac{1}{R_s + sL}\right)U_{Cp}(s) = \frac{E}{s}sC_T + \frac{U_{Cp}(0)}{s}sC_p - \frac{Li(0)}{R_s + sL} \tag{7}$$

$$U_{Cp}(s) = E\frac{sLC + R_sC - \frac{L}{R_s}}{s^2LC + s\left[R_sC + \frac{L}{R_p}\right] + 1 + \frac{R_s}{R_p}} \tag{8}$$

$$s_{1,2} = -\frac{\frac{L}{R_p} + R_sC}{2LC} \pm \sqrt{\left(\frac{\frac{L}{R_p} + R_sC}{2LC}\right)^2 - \frac{\frac{R_s}{R_p} + 1}{LC}} \tag{9}$$

Based on equations (8) and (9), a relation describing the voltage across the parasitic capacitor C_p after turning the transistor off, can be obtained.

When the switch is turning off (t_0), the voltage across the terminals of the inductor, and thereby at the internal capacitance C_p, can be expressed as following:

$$u_{Cp} = U_{Cp(0)} e^{-\alpha t} \cos \omega t, \tag{10}$$

where:

– damping factor α:

$$\alpha = \frac{\frac{L}{R_p} + R_s C}{2LC}; \tag{11}$$

– angular frequency ω:

$$\omega = \sqrt{\omega_0^2 - \alpha^2}; \tag{12}$$

– resonant angular frequency ω_0:

$$\omega_0 = \sqrt{\frac{\frac{R_s}{R_p} + 1}{LC}}; \tag{13}$$

– measured resultant capacitance C:

$$C = C_p + C_T + C_{sc}; \tag{14}$$

where C_T is the parasitic output capacitance of the transistor, and C_{sc} stands for the capacitance of voltage probe.

The obtained equations have been implemented in MATLAB to verify their correctness. The parameters of simulation have been listed in Table 1.

Table 1
Simulation parameters of winding and measurement circuit

No.	**Winding parameters**		
	Parameter	*unit*	*value*
1	Inductance, L	*mH*	1.2
2	Parasitic capacitance (assumed), C_p	*pF*	150
3	Series resistance, R_s	*mΩ*	100
4	Parallel resistance, R_p	*kΩ*	60
	Circuit parameters		
5	Supply voltage, E	*V*	10
6	Parasitic capacitance of transistor (from datasheet), C_T	*pF*	300
7	Probe capacitance, C_{sc}	*pF*	12

The results of the prepared simulation have been presented on Fig. 4. The resonant frequency of the observed waveform equals 217 kHz.

In practical approach, when a waveform of voltage across the inductor is observed, it is necessary to measure its period and the two next amplitudes of the observed damped oscillation. Then, the decrement of that damping can be calculated from:

$$\alpha = \frac{\ln(\frac{U_{Cp(0)}}{U_{Cp(nTs)}})}{nT_s}, \tag{15}$$

where n is the number of the next amplitude and T_s is the period of the damped oscillation (Fig. 4).

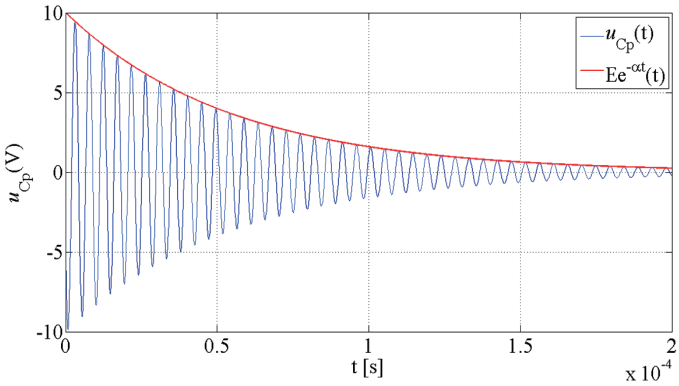

Fig. 4. Simulation results of the presented analytical description of damped resonance in the winding of an inductor

The series resistance of winding R_s is several orders of magnitude smaller than the parallel resistance R_p, so the ratio R_s/R_p from (13) can be neglected. Then, based on (12), the measured capacitance can be expresses by:

$$C = \frac{1}{((2\pi \frac{1}{T_s})^2 + \alpha^2)L}. \tag{16}$$

The value of coefficient α, obtained from (15), can be used for a possible correction of the parallel resistance R_p, which is a nonlinear parameter. To accurately estimate C, a precise determination of the value of inductance L is needed. During the presented experimental part, two methods of determining inductance have been used. The first method consisted of using a WK TMPRO 4230 type RLC meter, which returned a value of inductance equal to 1.1921 mH as a result of the measurement. The second method was based on a scope record during a voltage excitation (Fig. 5). During this test, a pulse of voltage was delivered to the inductor over a short time ($\Delta t = 27.9$ μs), and inductor current has been observed – the results are presented in Fig. 5. Based on the obtained results, a linearity of the changing current has been observed. Knowing the voltage level $U = 300$ V, the length of time pulse Δt, and the change

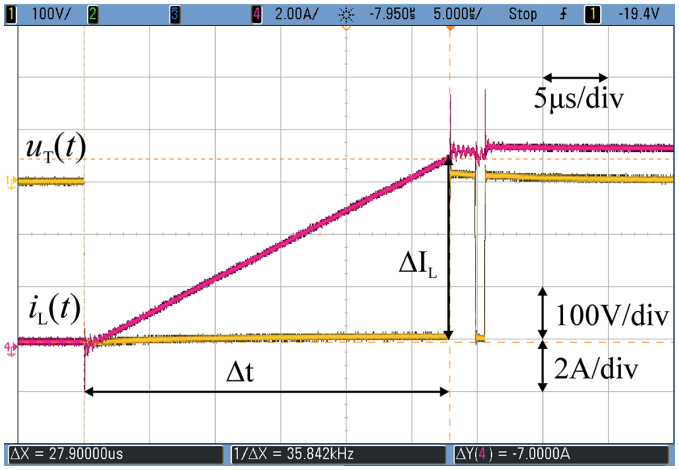

Fig. 5. Waveform of voltage across switch and current of the inductor during the inductance measurement process

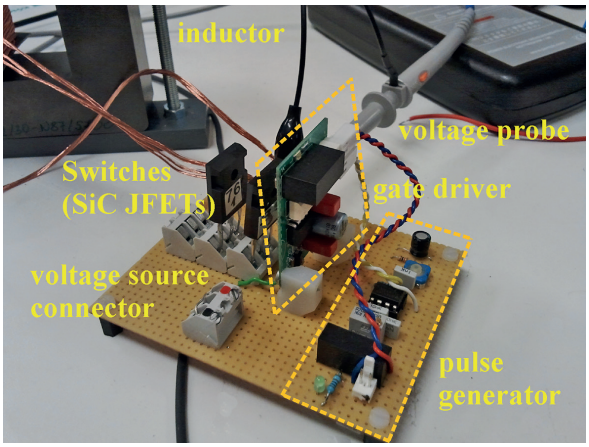

Fig. 6. The measurement setup

of inductor current ΔI_L, the inductance of the laboratory model can be calculated using:

$$L = \frac{U \cdot \Delta t}{\Delta I_L}. \tag{17}$$

Obtained result was equal 1.196 mH.

The next parameter of the measurement circuit, which is characterized by nonlinearity, is the output capacitance of the switch, which depends on drain-source voltage. Analytical determination of this parameter can be very complicated and difficult to estimate in experimental conditions. During the measurement tests, the parasitic capacitance of the switch (C_T) was estimated using a method where additional, identical transistors were used – in this case, three were selected. The capacitance of a single switch can be estimated by knowing the resultant capacitance of the circuit when a single transistor as a switch was used, and capacitance of a circuit where the same switch was connected in parallel with another one. Summarizing, six measurements were made. In the first three tests, a double switch as a parallel combination of two SiC JFETs has been used ($T_1||T_2$, $T_2||T_3$, $T_3||T_1$). In the next three tests, individual switches have been used (T_1, T_2, T_3). Knowing the resultant capacitance from these measurements, it was possible to estimate the individual output capacitance of the transistors:

$$C_{T1} = C_{31} - C_3 \tag{18}$$

$$C_{T2} = C_{12} - C_1 \tag{19}$$

$$C_{T3} = C_{23} - C_2 \tag{20}$$

where C_{T1}, C_{T2}, and C_{T3} are individual output capacitances of transistors T_1, T_2 and T_3; C_{12}, C_{23}, and C_{31} are the results of measurements and calculations performed using (14) in the case of double transistors in the circuit; C_1, C_2, and C_3 are the capacitances obtained from measurements and calculations using (14) with single-transistor switches. Fig. 7 shows an example of voltage waveforms obtained as a result of the laboratory tests.

Using the presented procedure, the parasitic capacitances have been measured, and the obtained values are: $C_{T1} = 302$ pF; $C_{T2} = 321$ pF, and $C_{T3} = 249$ pF. The value of voltage probe capacitance was obtained from the manufacturer ($C_{sc} = 12$ pF), and also by performing experiments ($C_{sc} = 11{,}25$ pF), which has been presented in [15] and [19].

Knowing the output capacitances of transistors, voltage probe, and the resultant capacitance of resonant circuit, calcu-

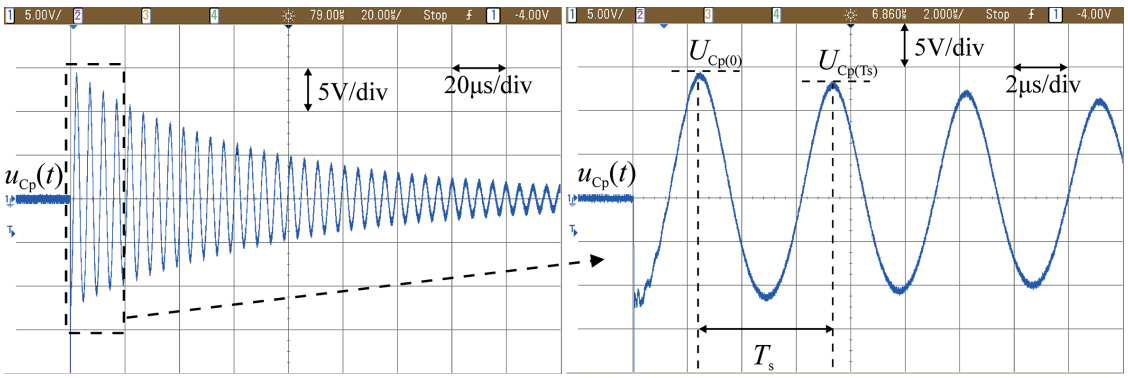

Fig. 7. Example of a waveform representing the voltage observed during the measurement

lated using (16), the parasitic capacitance of the winding can be estimated from:

$$C_p = C - C_T - C_{sc}. \tag{21}$$

The measured value is $C_{p(e)} = 155.33$ pF and it differs by 1.4 % from the value obtained by performing analytical calculations using (1–5):

$$\delta_{Cp} = \frac{C_{p(a)} - C_{p(e)}}{C_{p(a)}} 100\% \tag{22}$$

5. Summary

Determination of parasitic capacitance of inductor winding is very important in case of converters, where high dv/dt and high switching frequency are occurring. Reloading of currents of this capacitance takes place with each switching process in the transistors, which causes a rise in switching power losses, reducing the efficiency of a DC-DC converter. The results of the measurements presented in this paper, obtained through several tests, are very similar (the difference being less than 2%) and close to the results of analytical calculations. That level of accuracy creates an opportunity to estimate the parasitic capacitance of inductor winding during its design process. Moreover, the presented method of experimental measurement of parasitic capacitance is relatively easy to use and doesn`t require specialized measuring equipment.

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