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Layout Optimizations of Operational Amplifiers in Deep Submicron

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***Abstract*—Operational amplifies (op amps) are an integral part of many analog and mixed-signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from DC bias generation to high-speed amplification or filtering. The design of op amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. The thesis deals with the analysis, design and layout optimization of CMOS op amps in deep Submicron (DSM) from a study case. Finally, layout optimizations of op amps will be given, in which propose optimization techniques to mitigate these DSM effects in the place-and-route stage of VLSI physical design.**

***Keywords*—Layout Optimization, Deep Submicron (DSM), Operational Amplifier, place-and-route**

I. Introduce

An op amp is defined as a "high-gain differential amplifier.". By "high", it mean a value that is adequate for the application, typically in the range of 60dB to 120dB [1] . Since op amps usually employed to implement a feedback system, their open-loop gain is chosen according to the precision required of the closed-loop circuit.

Unlike traditional usages, most op amps were designed to serve as "general-purpose" building blocks, satisfying the requirements of many different application. Today's op amps design proceeds with the recognition that the trade-offs between the parameters eventually require a multi-dimensional compromise in overall implementation, making it necessary to know the adequate value that must be achieved for each parameter.

II. Performance Parameter

Open Loop Gain (OLG), Closed Loop Gain(CLG) & Gain BandWidth Product (GBWP) etc. will be concerned. The open-loop gain of an op amp determines the precision of the feedback system employing the op amp. The OLG is given as follow(1) when feedback is not introduced into the op amp circuit :

$$A_v = \frac{V_{out}}{V_{in}} \tag{1}$$

As shown in Fig.1, $\dot{A}$ denotes Open-Loop Gain of the op amp.$\dot{F}$ denotes feedback coefficient of the op amp, that is the reciprocal of ideal closed-loop gain, also characterizes multiple of reduction of characterization signal from $\dot{X}_o$ to $\dot{X}_f\dot{F}$=$\dot{A}\dot{F}$ denotes loop gain which the gain of the signal around the middle loop of Fig.1. Ideal CLG is 1/$\dot{A}$. Actual CLG is given as follow (2):

$$\dot{A}_{vF} = \frac{\dot{A}}{1 + \dot{A}\dot{F}} \tag{2}$$

The GBWP is an important parameter for any analog amplifier and it gives us an insight of the high frequency characteristics of that amplifier. The GBWP numerically is defined as the frequency at which the gain of the amplifier becomes equal to unity, that it is the product of gain and bandwidth.When the op amp is connected to the circuit in the form of negative feedback, the gain of the whole negative feedback network is lower than that of the open-loop gain. At this time, the GBWP of the closed-loop amplifier network is approximately equal to that of the open-loop amplifier network [2].According to S. Srinivasan: The frequency-dependent parameter characterizing the gain of op amps is the finite GBWP [3].

Trading with such parameters as speed and output voltage swings, the minimum required gain must therefore be known. A high OLG may also be necessary to suppress nonlinearity [4].

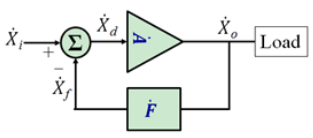
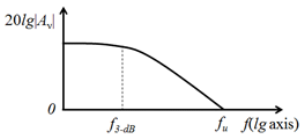


Fig. 1. Block diagram of negativeFig. 2. Gain roll-off with frequency feedback system



Small-Signal BandWidth (SSBW)

The high-frequency behavior of op amps plays a critical role in many applications. As the frequency of operation increase, the OLG begins to drop, creating larger errors in the feedback system. The SSBW is usually defined as the "unity-gain" frequency, fu. The 3-dB frequency, f3-dB, may also be specified to allow easier prediction of the closed-loop frequency response. And the small signal performance of CMOS op amps depend on the DC variable and geometric size of the device.

Large-Signal BandWidth (LSBW)

In many applications, op amps must operate with large transient signals. Under these conditions, nonlinear phenomena make it difficult to characterize the speed by merely small-signal properties such as the open-loop response.

Output Swing

Most system employing op amps require large voltage swings to accommodate a wide rang of signal amplitudes.

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A high-quality microphone that senses the music produced by an orchestra may generate instantaneous voltages that vary by more than four orders of magnitude, demanding that subsequent amplifiers and filters handle large swings (and/or achieve a low noise).

The need for large output swings has made fully differential op amps quite popular. Nonetheless, the maximum voltage swing trades with device size and bias current and hence speed. Achieving large swings is the principal challenge in today's op amp design.

Linearity

Open-loop op amps suffer from substantial nonlinearity. In the circuit of cascade op amp as shown in Fig.3, the input pair M1-M2 exhibits a nonlinear relationship between its differential drain current and input voltage. The issue of nonlinearity is tackled by two approaches: using fully differential implementations to suppress even-order harmonics and allowing sufficient open-loop gain such that closed-loop feedback system achieves adequate linearity. It is interesting to note in many feedback circuits, the linearity requirement, rather than the gain error requirement, governs the choice of the open-loop gain.

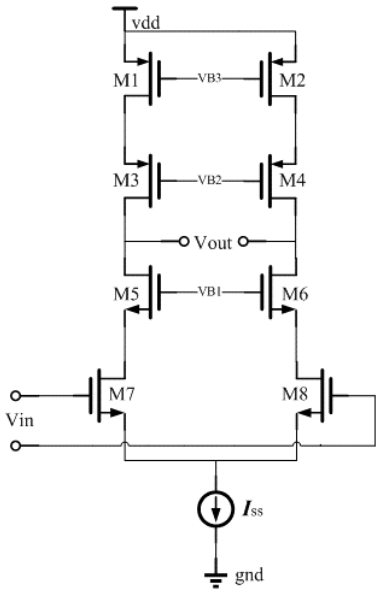

Fig. 3. Cascode op amp

Noise and Offset

The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality. In a typical op amp topology, several devices contribute noise and offset, necessitating large dimensions or boas currents. In the circuit of Fig.3, M1-M2 and M7-M8 contribute the most.

A trade-off between noise and output swing should also be recognized. For a given bias current, as the overdrive voltage of M7 and M8 in Fig.3 is lowered to allow larger swings at the output, their transconductance increases and so does their drain noise current.

Supply Rejection

Op amps are often employed in mixed-signal systems and sometimes connected to noisy digital supply lines. Thus, the performance of op amps in the presence of supply noise, especially as the noise frequency increases, is quite important. For this reason, fully differential topologies are preferred.

III. AN OP AMPS DESIGN

A. Design Approach for the Folded-Cascode Op Amp

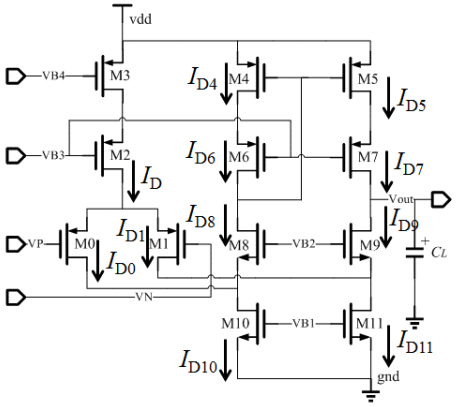

Fig. 4. A Folded Cascode Op Amp

The modelling of the folded-cascode Op Amp is shown in figure 4.

TABLE I
RESULTS OF SIMULATION.

Step	Relationship	Design Equation
1	Slew Rate	$SR = \frac{I_D}{C_L}$, $SR \geq 2\pi f V_m$, where f is the highest signal frequency, Hz, and V_m is the maximum peak voltage of the signal.
2	Bias Current in Output Cascode	$I_{D10} = I_{D11} = 1.2I_D$ to $1.5I_D$ Avoid Zero Current in Cascode
3	Maximum Output Voltage, $V_{out(max)}$	$S_{11}=\frac{2I_{D11}}{K'_N V^2_{DS11}}$, $S_9=\frac{2I_{D9}}{K'_N V^2_{DS9}}$, $Let\ \ S10=S11\ \ and\ \ S8=S9$ $V_{DS11}(sat)=V_{DS9}(sat)=\frac{V_{out(min)}-V_{gnd}}{2}$
4	Minimum Output Voltage, $V_{out(min)}$	$S_5=\frac{2I_{D5}}{K'_P V^2_{DS5}}$, $S_7=\frac{2I_{D7}}{K'_P V^2_{DS7}}$, $Let\ \ S4=S5\ \ and\ \ S6=S7$ $V_{DS7}(sat)=V_{DS5}(sat)=\frac{V_{DD}-V_{out(min)}}{2}$
5	GBWP	$GBWP=\frac{g_{m0}}{C_L}$, $S_0=S_1=\frac{g^2_{m0}}{K'_P I_D}=\frac{GBWP^2 C_L^2}{K'_P I_D}$
6	Minimum Input CM	$S_3=\frac{2I_D}{K'_P\left((V_P-V_N)_{min}-\sqrt{\frac{I_D}{K'_N S_0}}-V_{TH0}\right)^2}$
7	Maximum Input CM	$S_{10}=S_{11}=\frac{2I_{10}}{K'_N(V_{DD}-(V_P-V_N)_{min}+V_{TH0})^2}$
8	Differential Voltage Gain	$\lvert A_v\rvert=g_{m0}\left((g_{m8}r_{o3}(r_{o0}\lvert\rvert r_{o10})\right)\lvert\rvert(g_{m6}r_{o5}r_{o4})$
9	Power Dissipation	$P_{diss}=V_{DD}(I_D+I_{D4}+I_{D5})$

The design approach for the folded cascode op amp is shown in TABLE I.

Where K'_N or K'_P is the trans-conductance coefficient of NMOS or PMOS;
V_{TH0} is the threshold voltage of M0;
V_{DS5}, V_{DS7}, V_{DS9} or V_{DS11} is the drain-source voltage of M5, M7, M9 or M11;
g_{m0}, g_{m6} or g_{m8} is the trans-conductance of M0, M6 or M8;
r_{O0}, r_{O3}, r_{O4}, r_{O6} or r_{O10} is the output resistance of M0, M3, M4, M6 or M10 respectively.

The output swings of telescopic op amps are relatively limited. Another drawback of telescopic cascades is the difficulty in shorting their inputs and outputs. In order to alleviate the drawbacks of telescopic cascade op amps, namely, limited output swings and difficulty in shorting the input and output, a "folded cascade" op amp can be used [5].

B. A Folded-Cascode Op Amp Design and Simulation

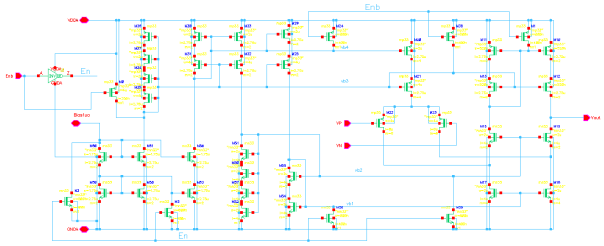

Fig. 5. A Realistic Folded-Cascode Op Amp Design

TABLE II
THE CHARACTERISTICS OF THE FOLDED-CASCODE OP AMP.

Characteristics	Symbol	Specification Values	Simulation Values
Open-Loop Gain	OLG	$> 80dB$	88.9dB
Gain Bandwidth Product	GBWP	10MHz	10.2MHz
Phase Margin	PM	$> 60°$	89°
Common Mode Rejection Ratio	CMRR	$> 80dB$	83dB
Power Supply Rejection Ratio	PSRR	$> 70dB$	78dB
Load Capacitance		1pF	

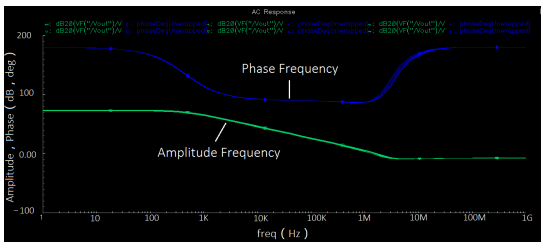

Fig. 6. AC Gain & Phase

A realistic folded-cascode op amp design is showed in Fig.5. And the main characteristics of the Folded-Cascode Op Amp are shown in Table II. AC gain & phase are shown in Fig.6. In the Fig.7 & Fig.8 are CMRR and PSRR waveforms respectively.

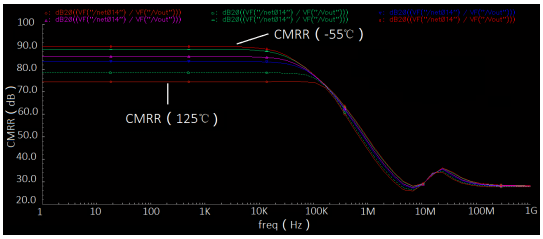

Fig. 7. Simulation Waveform of Common Mode Rejection Ratio (CMRR)

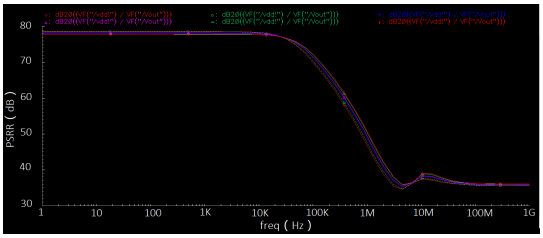

Fig. 8. Simulation Waveform of Power Supply Rejection Ratio (PSRR)

IV. THE FOLDED-CASCODE OP AMP LAYOUT & PHYSICAL POST-SIMULATIONS

Layout design and verification of the Folded-Cascode Op Amp based on0.18um process as showed in Fig.9.

And by extracting RC parasitic parameters of layout, a circuit view file called "caliber_RC" is obtained. Then the circuit is simulated, and the simulation results are as follows.

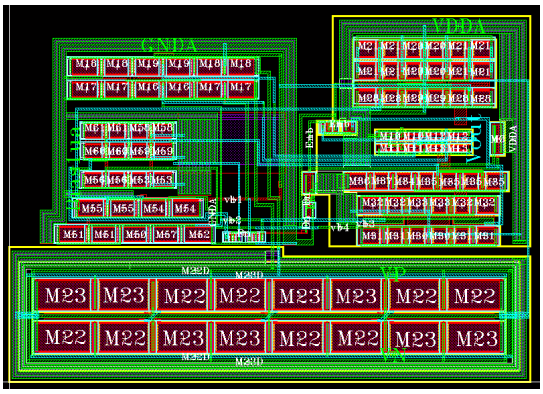

Fig. 9. Simulation Waveform of Power Supply Rejection Ratio (PSRR)

A. Power Supply Rejection Ratio (PSRR)

Physical post-simulations waveforms of PSRR with red circle is showed in Fig.10. The sampling points are $-55°C$, $-40°C$, $0°C$, $27°C$, $85°C$, $125°C$, PSRR is between 77db and 78dB, and PSRR is basically stable with the increase of temperature. Compared with the former simulation, as

showed in Fig.8 and square mark in Fig.10, first PSRR is lower than the former simulation, at the same time, the effective frequency drops below 100Hz (as shown in TABLE III), and the curve moves to the left.

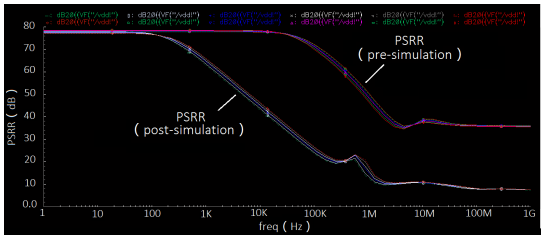

Fig. 10. The comparison of Pre and post simulation waveforms (PSRR)

TABLE III
PARAMETER TABLE OF PSRR POST SIMULATION.

Temperature sampling($^\circ C$)	-55	-40	0	27	85	125
PSRR(dB)	$77 \sim 78 \quad (< 100Hz)$					
CMRR(dB)	89.6	88.3	85.7	82.8	77.6	73.4
Main Pole(-3dB)	73.9	73.8	73.5	73.3	72.7	72.3
Amplitude Frequency Gain(dB)	$63 \sim 66$					

B. Power Supply Rejection Ratio (PSRR)

In Fig.11, a group of red circle waveforms are post-simulation waveforms. The sampling temperatures are $-55^\circ C$, $-40^\circ C$, $0^\circ C$, $27^\circ C$, $85^\circ C$, $125^\circ C$, and CMRR decreases with the increase of temperature. Compared with the pre-simulation, the post-simulation CMRR is lower, while the effective frequency drops to $1kHz \sim 5KHz$, and the curve moves down to the left. The pre-simulation dB is between 74dB and 90dB, and the latter is between 73db and 89dB (as shown in TABLE IV.

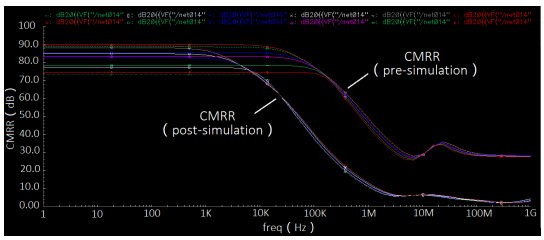

Fig. 11. Comparison of CMRR Pre-simulation and Post-Simulation Waveforms

C. Frequency Characteristic

The post-simulation of frequency characteristics is shown in TABLE V. Generally, the phase margin is the major change, and the rest changes little. As shown in Fig.12, the phase frequency (PF) characteristics and Amplitude Frequency (AF)

TABLE IV
PARAMETER TABLE OF PSRR POST SIMULATION.

Temperature sampling($^\circ C$)	-55	-40	0	27	85	125
Maximum CMRR (Pre-simulation)(dB)	90.1	88.9	85.7	83.5	78.6	74.5
Maximum CMRR (post-simulation)(dB)	89.6	88.3	85.7	82.8	77.6	73.4

Characteristicsof the pre-simulation & Post-simulation are indicated.

As shown in Fig.12, when the phase margin is 0dB, the phase margin changes greatly from 90 degrees to $54.66^\circ C$, and the best range of $45^\circ C \sim 60^\circ C$ expected by the project is obtained.

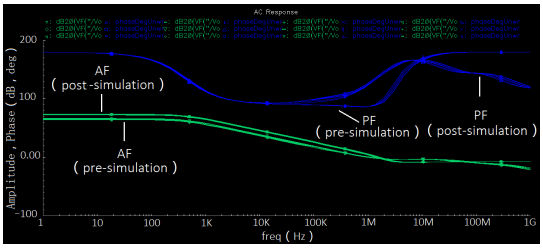

Fig. 12. Phase Frequency(PF) Characteristics and Amplitude Frequency(AF) Characteristics of the Pre-Simulation & Post-Simulation

TABLE V
POST-SIMULATION FREQUENCY CHARACTERISTIC PARAMETER TABL.

Temperature sampling($^\circ C$)	-55	-40	0	27	85	125
Phase Margin (Pre-Simulation)($^\circ$)	92.5	92.5	92	90.7	91	90.4
Phase Margin (Post-Simulation)	54.66°					
Main Pole(-3dB)($^\circ C$)	45	45	45	45	45	45
Amplitude Frequency Gain (Pre-Simulation)(dB)	73.9	73.8	73.5	73.3	72.7	72.3
Amplitude Frequency Gain (Post-Simulation)	$63dB \sim 66dB$					

V. EFFECTS OF LAYOUT ON OP AMP PERFORMANCE AND LAYOUT OPTIMIZATIONS

It is significant to reduce the parasitic effect of physical layout on the performance of op amp.It can be seen that there are a large number of articles that propose algorithms for DSM layout optimization [6]–[14]. However, These articles are all algorithmic modeling, and do not analyze cases. In this paper, the layout and wiring layout of op amp are optimized, and the

case study and analysis are attempted to obtain guidance for layout design. Optimize the layout design of op amp cases, so as to guide layout engineers to design layout.

A. Placement Design

The variability of circuit delay due to device and interconnect variation (eg. Gate length, oxide thickness, threshold voltage and interconnect width variations) has become a great concern.The equivalent circuit of the simplified MOS (Metal Oxide Semiconductor)is shown in Figure 13. Where C_{GD} denotes Gate-Drain capacitance, C_{GS} Gate-Source capacitance, r_D Drain-output resistance, C_O Drain-Source capacitance, $g_m \left(= \frac{dI_{DS}}{dU_{DS}}|_{U_{DS}-const}\right)$ trans-conductance, U_{GS} Voltage applied to the gate. According to the definition of cut-off frequency, there is an equation as formula (3).

$$U_{GS}C_{GS}\omega_T = g_m U_{GS} \tag{3}$$

And known $\omega_T = 2\pi f_T$,The cut-off frequency as shown in formula (4) can be obtained by equation (1). And when MOS is in the saturation, f_T is as fallow.

$$f_T = \frac{g_m}{2\pi C_{GS}} = \frac{3\mu_n}{2\pi L^2}(U_{GS} - U_T) \tag{4}$$

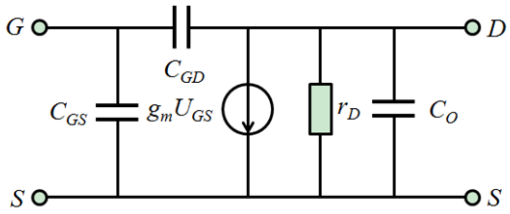

Fig. 13. The equivalent circuit of the simplified MOS

If device channel $L = L_1 + L_2$, then there are equations (5),(6) and (7) as fallow. The derived inequality is shown in formula (8).

$$f_T = \frac{3\mu_n}{2\pi (L_1 + L_2)^2}(U_{GS} - U_T) \tag{5}$$

$$f_{T1} = \frac{3\mu_n}{2\pi L_1^2}(U_{GS} - U_T) \tag{6}$$

$$f_{T2} = \frac{3\mu_n}{2\pi L_2^2}(U_{GS} - U_T) \tag{7}$$

$$f_T < f_{T1} + f_{T2} \tag{8}$$

The results show that the device with channel length l can be divided into two devices with channel length L_1 and L_2 in series, so as to obtain better cut-off frequency.MOS with channel length l can be equivalent to two MOSs in series with channel length L_1 and L_2 as shown in Fig.14.

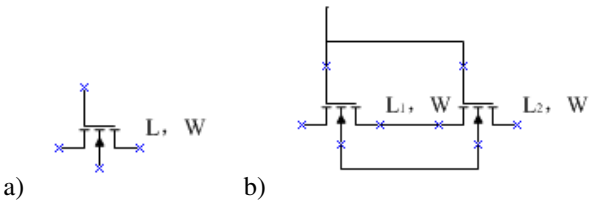

Fig. 14. Circuit (a) is equivalent to circuit (b). (a) MOS with channel length L and width W. (b)two MOSs in series with channel length L_1 and L_2

B. Interconnect Optimization for Path Length Minimization

Coupling capacitance (crosstalk) has become one of the most critical issues in Deep Submicron (DSM) physical design [11]. The OP Amp layout isn't optimized as shown in Fig.9.Although the temperature has little effect on the performance of Op Amp, the post-simulation frequency characteristic is not good. As a result, in the deep submicron, the interconnect has to be modeled as a distributed RC or RLC circuit [6]–[14].

The interconnection of a net consists of a set of wire segments (often in multiple routing layers) connecting all the pins in the net. It can be represented by a graph, in which each edge denotes a wire segment and each vertex denotes a pin or joint of two wire segments. Interconnects are generally rectilinear.

Research on the construction of Minimum Spanning Trees (MST) and Steiner Minimal Trees (SMT) is directly applicable to problems in Op Amp interconnect design.The MST problem involves finding a set of edges E which connect a given set of points P with minimum total cost. While improvement of an MST through edge merging can be effective at minimizing tree length on average, there exist pathological cases in which merge-based Steiner heuristics can exhibit the worst case performance [15].

In the paper, the Manhattan (rectilinear) distance metrics are being mainly concerned with. The Manhattan distance between points u and v is used d(u,v) to denote. If edge e connects u and v, then $|e| \geq d(u, v)$. The cost of edge e refers to its wirelength, and is denoted by $|e|$, with the width of edge e denoted by we, the cost of edge e may refer to its ares. $|T|$ denotes the cost of all edges in tree T. Let t(u,v) denote the signal delay from node u to node v. Let r, ca and cf denote the unit square wire resistance, unit capacitance, and unit length fringing capacitance (for 2 sides), respectively. Then the wire resistance of edge e, denoted re, and the total wire capacitance of e, denoted ce, are given as follows (9):

$$r_e = \frac{r \cdot |e|}{w_e}, \quad C_e = C_a \cdot |e| \cdot w_e + C_f \cdot |e| \tag{9}$$

While improvement of an MST through edge merging can be effective at minimizing tree length on average, there exist pathological cases in which merge-based Steiner heuristics can exhibit the worst case performance. As shown in Figure 15, one such case is shown. The most common form of node connection in the circuit is shown in Figure 15 (a). Traditional layout wiring is likely to be connected node from

the beginning to the end in Fig.15 (b), so the maximum delay of the signal is 5 units, but is 2 units if optimized Steiner tree is used in Fig.15 (c). The optimized Steiner tree is significant for reducing delay.

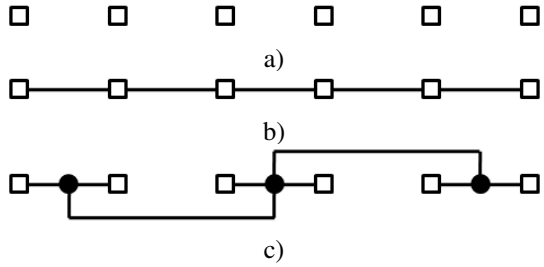

Fig. 15. A pathological case for conventional merge-based Steiner tree heuristics. (a) A difficult problem for merge-based Steiner heuristics. (b) A traditional merge-based Spanning Tree. (c) The optimal Steiner tree solution

VI. LAYOUT OPTIMIZATIONS AND EFFECTS OF LAYOUT ON OP AMP PERFORMANCE

A. *Op Amp Layout Optimizations*

The analysis of operational amplifier circuit is shown in Figure 16. The top half of the circuit is PMOS devices and the bottom half is NMOS devices, in which include mirror current source unit, series MOS and differential pair. PMOS and NMOS device nodes and their interconnection diagram are extracted as shown in Figure 17. The v3 interconnection in Figure 17 has a similar structure to that in Figure 15 (b), the v4 is a 4-node structure in which. Their maximum delay is 5 units and 3 units respectively. This case uses the optimized Steiner tree as shown in Figure 18 in which v3 reduces the maximum delay to 2 units, v4 to 1 unit as shown in Fig.19.

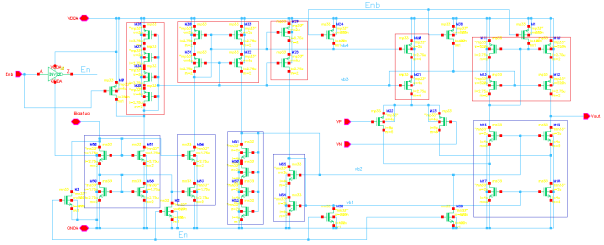

Fig. 16. Op Amp is divided into modules

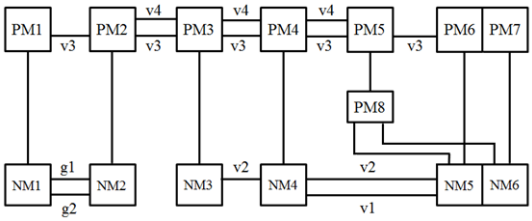

Fig. 17. Op Amp is divided into modules

The module placement takes the shortest signal wiring as the main consideration, and does not take the long line as far

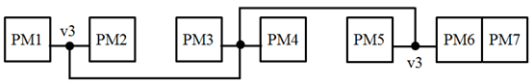

Fig. 18. Op Amp is divided into modules

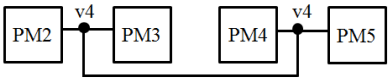

Fig. 19. Op Amp is divided into modules

as possible to reduce the parasitic resistance and capacitance. Considering that there is a MOS series circuit similar to Figure 14 in the operational amplifier circuit, reducing the channel length can effectively improve the frequency characteristics of the device.

B. *Effects of Layout on Op Amp Performance*

After layout and wiring optimization, the layout of the operational amplifier is shown in Fig.20. Then We do physical post simulation of the layout. In other words, the circuit is extracted from the layout, and then Power Supply Rejection Ratio (PSRR), Common Mode Rejection Ratio (CMRR) and Amplitude frequency & phase frequency characteristics are simulated. The simulation results before and after layout physics are compared as follows:

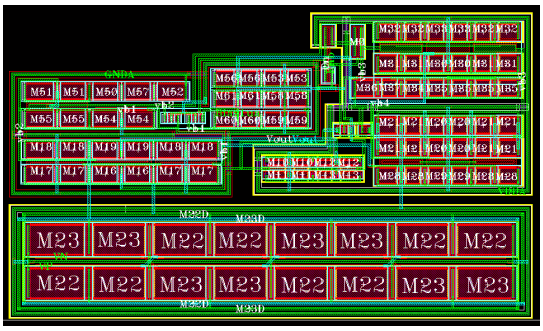

Fig. 20. Layout optimization of operational amplifier

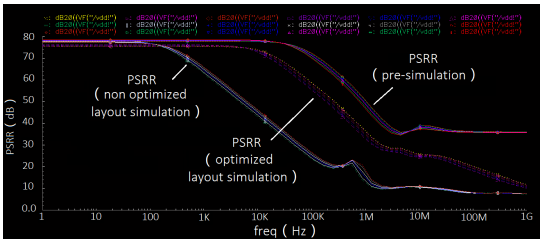

Fig. 21. Comparison of PSRR pre simulation, non optimized layout physical post simulation and optimized layout physical post simulation

As shown in Figure 21, the results of PSRR power supply suppression pre simulation, non optimized layout physical post simulation and optimized layout physical post simulation

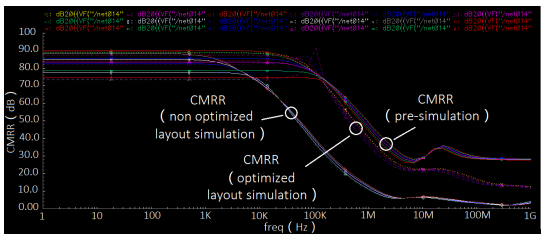

Fig. 22. Comparison of CMRR pre simulation, non optimized layout post simulation and optimized layout post simulation

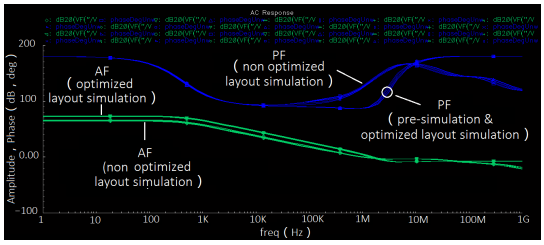

Fig. 23. Comparison of simulation results of amplitude frequency(AF) & phase frequency(PF) characteristics, physical simulation of non optimized layout and physical simulation of optimized layout

are compared. It can be found that the PSRR characteristic curve is improved significantly after layout and wiring optimization. PSRR simulation sampling temperature range $125°C \sim -55°C$.

As shown in Figure 22, the results of CMRR common mode rejection pre simulation, non optimized layout physical post simulation and optimized layout physical post simulation are compared. It can be found that after layout and routing optimization, the CMRR characteristic curve is significantly improved. CMRR simulation sampling temperature range $125°C \sim -55°C$.

As shown in Figure 23, the results of simulation before amplitude frequency characteristics and phase frequency characteristics, physical simulation after layout optimization and physical simulation after layout optimization are compared. It can be found that after layout and routing optimization, the amplitude frequency and phase frequency characteristics are almost coincident with the pre simulation curve, which shows that the optimized layout can basically keep the pre simulation characteristics unchanged.

In conclusion, in the deep submicron environment, the layout and routing optimization can improve the performance of op amp significantly: PSRR, CMRR, amplitude frequency and phase frequency characteristics, especially the frequency characteristics of op amp are not affected too much by layout.

VII. CONCLUSION

Because there are many mirror current source configurations in Op Amp Circuits, for the interconnection as shown in Figure 15, we can abandon the traditional head-to-tail wiring and adopt the optimized Steiner tree. The maximum interconnect delay can be reduced to 2 or 1 interconnect unit. The module placement should be considered of the shortest distance from one module to another in terms of signal. Two modules connected by signal can be placed close to each other to reduce the delay and frequency loss caused by parasitic R and C pairs. The channel length of the device can also be reduced by the equivalent transformation of the device to obtain good frequency characteristics. The simulation results show that this layout optimization technology can greatly improve many performance parameters of op amp, and these optimization technologies can also be used in other similar circuit layout design. The post simulation of op amp layout shows that the working frequency is obviously reduced, and the phase margin is $54.66°$ in the post simulation, which has a good engineering value.This paper uses post-simulation to optimize the performance of op amp through layout and wiring design.

RELATION TO PRIOR WORK

Recently a LDO (Low Dropout Linear Regulator) layout of SOC is designed based on $0.13\mu m$. The ESD protective device is using the GGNMOS designed according to this work. At last we will research for ESD characteristics biased on nan-meter process.

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