Metrol. Meas. Syst., Vol. 28 (2021) No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

PAN POLSKA AKADEMIA NAUK

METROLOGY AND MEASUREMENT SYSTEMS
Index 330930, ISSN 0860-8229
www.metrology.wat.edu.pl

M&MS

JITTER GENERATION MODEL BASED ON TIMING MODULATION AND CROSS POINT CALIBRATION FOR JITTER DECOMPOSITION

Nan Ren, Zaiming Fu, Shengcun Lei, Hanglin Liu, Shulin Tian

University of Electronic Science and Technology of China, School of Automation Engineering, Chengdu 611731, China
(*rennan@uestc.edu.cn*, ✉ *fuzaimin@163.com*, +86 6183 1321, *lsc1995thoralex@163.com*, *lnlhlzr@163.com*, *shulin@uestc.edu.cn*)

Abstract

High-speed serial standards are rapidly developing, and with a requirement for effective compliance and characterization measurement methods. Jitter decomposition consists in troubleshooting steps based on jitter components from decomposition results. In order to verify algorithms with different deterministic jitter (DJ) in actual circuits, jitter generation model by cross-point calibration and timing modulation for jitter decomposition is presented in this paper. The generated jitter is pre-processed by cross-point calibration which improves the accuracy of jitter generation. Precisely controllable DJ and random jitter (RJ) are generated by timing modulation such as data-dependent jitter (DDJ), duty cycle distortion (DCD), bounded uncorrelated jitter (BUJ), and period jitter (PJ). The benefit of the cross-point calibration was verified by comparing generation of controllable jitter with and without cross-point calibration. The accuracy and advantage of the proposed method were demonstrated by comparing with the method of jitter generation by analog modulation. Then, the validity of the proposed method was demonstrated by hardware experiments where the jitter frequency had an accuracy of ±20 ppm, the jitter amplitude ranged from 10 ps to 8.33 ns, a step of 2 ps or 10 ps, and jitter amplitude was independent of jitter frequency and data rate.

Keywords: jitter decomposition, jitter generation, cross-point calibration, timing modulation, deterministic jitter and random jitter.

1. Introduction

New high-speed serial data standards have emerged such as *universal serial bus* (USB) and the *peripheral components interconnect express* (PCIE). These serial standards are more susceptible to jitter and significantly cause *bit error rate* (BER) [1, 2], and all this with the requirement for effective compliance and characterization measurement [3, 4]. Jitter decomposition consists in troubleshooting steps based on jitter components from decomposition results [5–7]. The existing jitter decomposition algorithms verify the accuracy by simulation calculation [8–11] or by generating jitter through analog modulation [12, 13]. The *deterministic jitter* (DJ) generated

Article history: received May 10, 2020; revised September 27, 2020; accepted October 26, 2020; available online December 14, 2021.

in actual circuit needs to be considered in the case of *data-dependent jitter* (DDJ), *duty cycle distortion* (DCD), *bounded uncorrelated jitter* (BUJ), and *period jitter* (PJ). However, in the verification of simulation calculation, only the dual Dirac jitter is considered, and in another verification method, the DCD jitter cannot be generated as the generated jitter by this verification method has low accuracy. Therefore, it is necessary to generate a different DJ that has known and controllable amplitude and frequency for verifying algorithms of jitter decomposition. Jitter generation can also perform jitter tolerance [14], detect the BER of the code stream [15], reduce interference [16], improve the linearity of the CDR *phase detector* (PD) [17], *etc*.

Analog modulation methods for jitter generation are described which use an independent signal source as a modulation signal to modulate the clock source, then uses the modulated clock as the clock input of the data generator, and finally generates the jittery data pattern [18–20]. It is easy to introduce noise in analog modulation and the instrument limits its accuracy and practicability. Li Y. *et al.* described a jitter generation method based on modulation, and it is necessary to design a complex low-pass filter to filter high-frequency quantization noise However, this filter is useless when the frequency of the data signal is high [21]. Ispir M. *et al.* proposed a method of generating real-time colored random jitter using *inverse Fourier transform* (IFFT), and verified the adjustment of a single random jitter through an experimental circuit [22]. This method provides a theoretical basis for generating different random jitter. Bidaj K. *et al.* proposed a method for generating random jitter on data pattern with a Gaussian distribution from a colored noise *power spectral density* (PSD) distribution using a *cumulative distribution function* (CDF) and a *complementary cumulative density function* (CCDF). However, this method studies only the unbounded and uncorrelated jitter generation method and does not study deterministic jitter generation [23, 28]; Xia T. *et al.* proposed a phase deviation generation program to inject controllable jitter into the clock signal [24], but this method uses oversampling and cannot be applied to high-speed digital systems. Jovanovic G. *et al.* proposed using a voltage-controlled delay line to generate different jitter profiles where it is used as a voltage-controlled oscillator of the *digital phase locked loop* (DPLL) to generate the final jittery clock signal. It is also the method of modulation [25, 26]. Calbaza D.E. *et al.* described the jitter generated by *direct digital synthesis* (DDS) and provided a theoretical basis for jitter generation [27]. A jitter generation method using cross-point calibration and timing modulation is presented in this paper to resolve the following issues:

(1) The control of jitter amplitude of the jitter generation method based on analog modulation is limited to the jitter frequency. We expect both the jitter frequency and amplitude to be freely controllable;
(2) The carrier signal of modulation is limited by the bandwidth We expect the original data pattern not to be limited by the filter;
(3) The existing jitter generation method cannot produce the superposition of different jitter profiles and cannot simulate the complex jitter that exists in the circuit;
(4) Introducing the calibration method to further improve accuracy;
(5) Providing an experimental test bench for the jitter decomposition algorithm.

2. Timing interval error jitter

Jitter can be divided into relative jitter, period jitter and *time interval error* (TIE) jitter. Relative jitter is the deviation of an actual signal from another non-ideal clock. Period jitter is the difference between the period of the actual signal and the ideal clock. TIE Jitter refers to

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

the short-term variation of the digital signal from the ideal positions at an important point in time [29] It can also refer to deviation of the actual signal from the edge of the ideal signal, that is, the deviation of the time of the signal [30]. In this paper, TIE jitter is used as a standard for measuring jitter.

An oscilloscope used for testing can directly measure the TIE Track. TIE was initially defined in the G.810 Recommendation issued by the Telecommunication Standardization Sector of the International Telecommunication Union [31]. It has since been widely used as a basic unit for analyzing data jitter in test instrument [32]. In a high-speed serial data system, TIE jitter refers to the phase difference between the edge of the data signal and the edge of the clock signal as shown in Fig. 1.

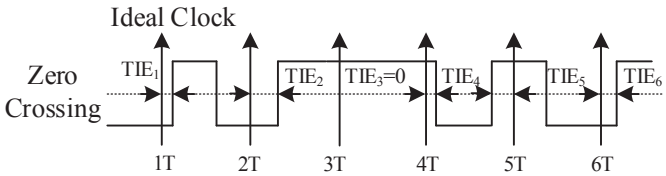


Fig. 1. Time interval error (TIE) [39].

As shown in Fig. 1, TIE_1 and TIE_2 are relative phase differences between the data signal and the clock, respectively, and this is TIE jitter [33].

$$\mathrm{TIE}_k = t_{Dk} - t_{Ck}\,, \tag{1}$$

where t_{Ck} is time of each rising edge of the clock and t_{Dk} is time of the data edge position corresponding t_{Ck}.

Total jitter (TJ) can be divided into *deterministic jitter* (DJ) and *random jitter* (RJ), where RJ is unbounded uncorrelated jitter, DJ is bounded jitter. DJ can be further divided into *data-dependent jitter* (DDJ) and *data-independent jitter* (DIJ), where DDJ can be divided into *duty cycle distortion* (DCD) and *Intersymbol interference* (ISI) and DIJ can be divided into *bounded uncorrelated jitter* (BUJ) and *period jitter* (PJ) [34].

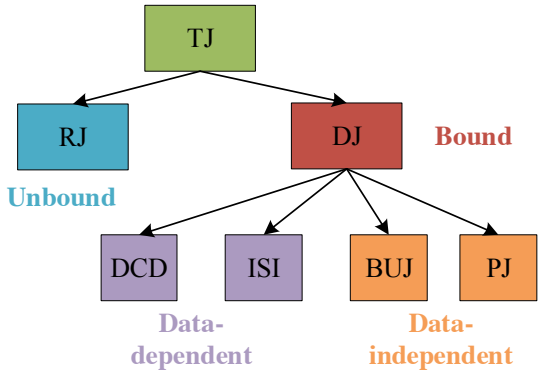


Fig. 2. The type of jitter.

3. Jitter model

In order to perform jitter decomposition, the dual-Dirac, sinusoidal, uniform, triangular jitter, and RJ are used. The dual-Dirac jitter may be caused by DCD, the sinusoidal jitter (SJ) can be caused by PJ, the uniform jitter may be caused by ISI and the triangular jitter can be caused by BUJ. The mathematical expressions of these jitters are given in this paper and they are convenient for mutual verification with the TIE Track and histogram measured with the oscilloscope [8].

3.1. Sinusoidal jitter

Sinusoidal jitter is uncorrelated with the data signal. It is caused by adjacent circuits such as power supplies, on-chip oscillators, data buses, *etc*. It is often used for jitter tolerance testing. Here, a sinusoidal jitter is given in the following equation [35]:

$$\begin{aligned}\Delta t_{\mathrm{SIN}}[n] &= A\sin\left(2\pi f_0(t-nT)+\Phi\right)\\ &= a\sin\left(\frac{2\pi f_0 n}{f_s}\right)+b\cos\left(\frac{2\pi f_0 n}{f_s}\right),\end{aligned} \tag{2}$$

where $\Delta t_{\mathrm{SIN}}[n]$ is sinusoidal jitter amount at sampling time nT, f_0 represents the frequency of sinusoidal jitter and A is amplitude of sinusoidal jitter.

3.2. Uniform jitter

ISI can give rise to uniform jitter. The mathematical model of uniform jitter is given in the following equation:

$$\Delta t_{\mathrm{tri}}[n] = \begin{cases} \dfrac{2A_{\mathrm{tri}}}{\tau}t + A_{tri} & -\dfrac{\tau}{2}+nT \le t \le nT \\ -\dfrac{2A_{\mathrm{tri}}}{\tau}t + A_{tri} & nT \le t \le \dfrac{\tau}{2}+nT \end{cases}, \tag{3}$$

where $\Delta t_{\mathrm{tri}}[n]$ is uniform jitter at the sampling time nT, A_{tri} is amplitude of uniform jitter.

3.3. DCD jitter

DCD is an important deterministic jitter. It is caused by non-idealities such as asymmetric rising and falling edges of the path and it is half of the data rate which can be modeled as [34]:

$$\begin{aligned}\Delta t_{\mathrm{DCD}}[n] &= J_{\mathrm{DCD}} \times \cos(n\pi)\\ &= [-J_{\mathrm{DCD}}, J_{\mathrm{DCD}}, -J_{\mathrm{DCD}}, J_{\mathrm{DCD}}, \ldots],\end{aligned} \tag{4}$$

where $\Delta t_{\mathrm{DCD}}[n]$ is the DCD at the sampling time nT, and J_{DCD} is amplitude of the DCD.

3.4. BUJ jitter

BUJ can cause the rectangular jitter. The mathematical model of the rectangular jitter is given in the following equation:

$$\Delta t_{\mathrm{rect}}[n] = A_{\mathrm{rect}} \times \mathrm{sgn}[\sin(2\pi f_j nT)], \tag{5}$$

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

where nT is sampling time of the uniform jitter, A_{rect} is amplitude of the BUJ jitter, f_j is frequency of the BUJ jitter, and sgn[•] rectangular wave function:

$$\text{sgn}[T] = \begin{cases} 1 & T \geq 0 \\ -1 & T < 0 \end{cases} . \tag{6}$$

3.5. Random jitter

RJ is caused by thermal noise, shot noise, and other high-order noise. It can be created with Gaussian white noise. And the statistical *probability density function* (PDF) for RJ is given in [36]:

$$f_{\text{RJ}}(\Delta t) = \frac{1}{\sqrt{2\pi\sigma}} \exp - \frac{(\Delta t - \mu)^2}{2\sigma^2}, \tag{7}$$

where $f_{\text{RJ}}(\Delta t)$ is RJ amplitude of data bit n at sample time nT, μ is mean of RJ and σ is standard deviation of RJ. In this method σ can be adjusted.

4. Jitter generation model

This section gives details of the jitter generation model as shown in Fig. 3, including cross-point calibration, the timing modulation method, delay compensation and jitter synthesis. In subsection 4.1, cross-point calibration method is proposed. In subsection 4.2, the timing modulation method, delay compensation, and jitter synthesis are proposed where, timing modulation includes single jitter generation, random jitter generation and mixed jitter generation.

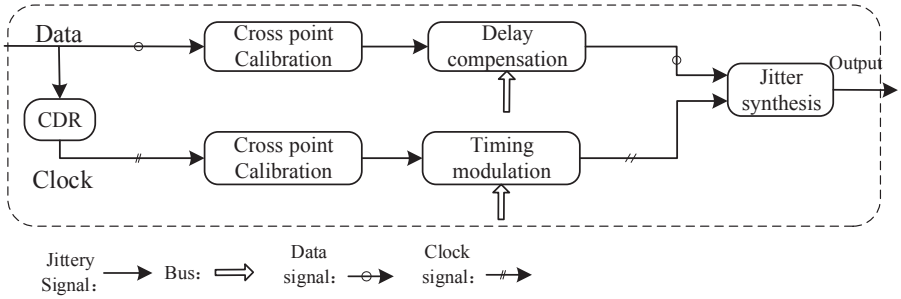


Fig. 3. Timing modulation and cross point calibration method for jitter generation.

4.1. Cross point calibration

The cross-point of the eye diagram percentage relationship can express the ability of different signals "1" and "0" to transmit signal quality, as well as relationship between different signal width and cross-point percentages. The cross-point is calculated according to the vertical statistical center of the average. The proportional equation is as follows [37]:

$$\textit{Cross point of the eye diagram percentage} = \frac{(\textit{Cross point level} - \textit{'0' level})}{(\textit{'1' level} - \textit{'0' level})} \times 100\%. \tag{8}$$

This paper proposes a cross point calibration method to tune the generated jitter amplitude which reconstructs the data pattern by changing the relative delay of the rising edge and the falling edge without changing the slew rate of the data pattern.

The cross-point calibration includes an input buffer, a digital control delay circuit, and output driver as shown in Fig. 4. The input buffer is a fan-out buffer, which can divide input data into two data, one is rising data and the other is falling data. The digital control delay circuit is divided into two programmable delay lines, an AND logic gate, an OR logic gate, and a multiplexer. The programmable delay line can accurately control the delay value of the signal. The signal can be reconstructed by the difference of the delay of the rising data and the falling data. When the cross point is greater than 50%, the two delay signals are passed through the AND gate to achieve cross-point calibration and reconstruct the data pattern. Conversely, when the cross point is less than 50%, the OR gate is used to calibrate. The multiplexer performs output selection. The output drive enhances the drive capability of the signal and creates a cross point at the desired location.

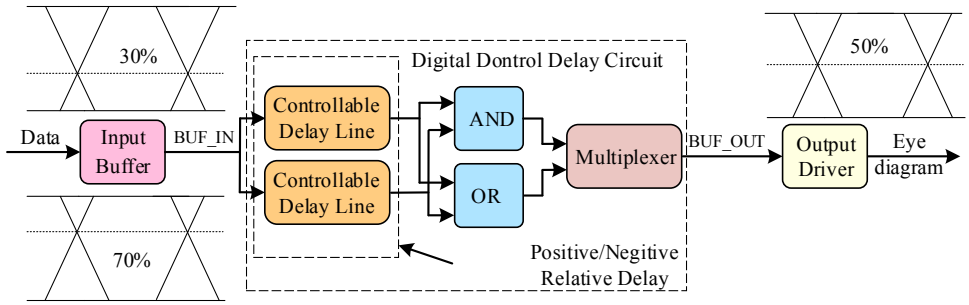


Fig. 4. The cross-point calibration method.

Figure 5 gives a specifies example of cross-point calibration when the cross point is greater than 50%. The input signal is fanned out into two signals through the input buffer and then is sent to the programmable delay line. Signal A is the original signal. Signal A_{td} is the signal delayed by T_d. They are the ADD gate and Signal A_{AND} is the output of this gate. So, the AND digital logic can realize the downward shift of eye diagram of the output signal, thereby adjusting the signal cross point. Conversely, OR logic can realize the cross-point calibration when the cross point is less than 50%.

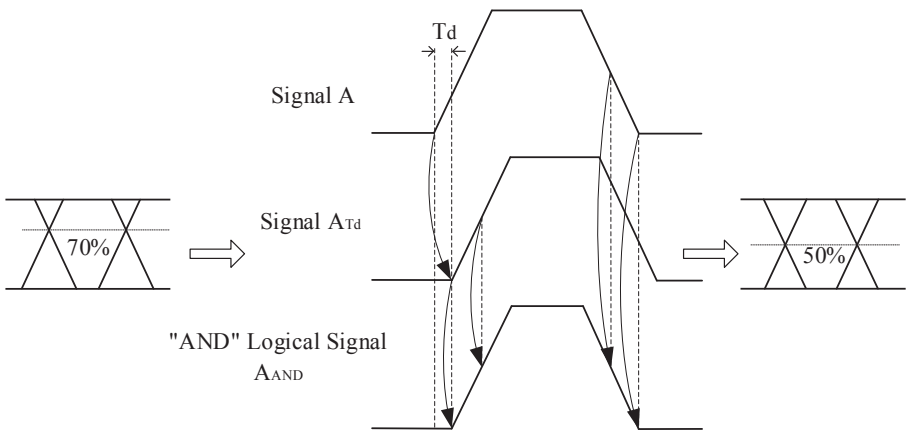


Fig. 5. Calibrate cross point time sequence diagram.

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

The timing diagram is shown in Fig. 6.

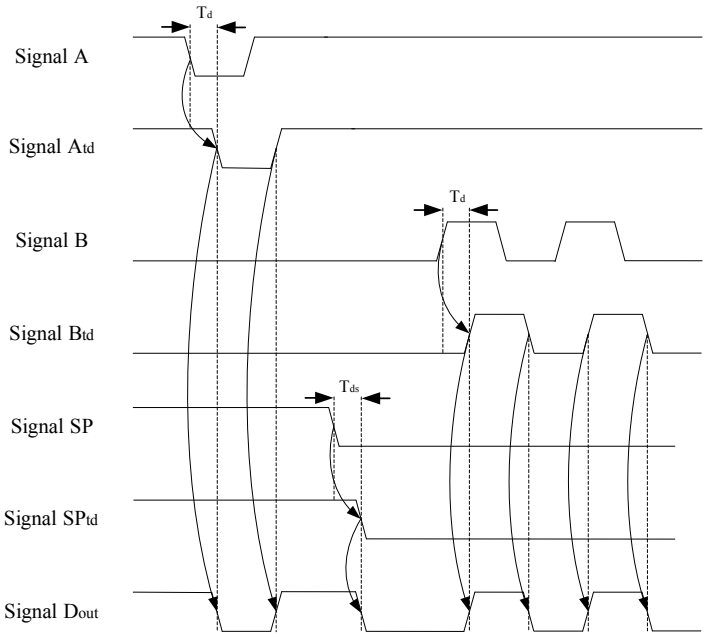


Fig. 6. The timing diagram of cross point calibration.

4.2. Timing modulation

The timing modulation method as shown in Fig. 7 realizes precise and controllable jitter generation. It mainly includes *clock data recovery* (CDR), cross-point calibration, timing modulation, delay compensation and jitter synthesis. It also includes a control system that provides a complete hardware platform for stable operation of the software system and provides control resources for jitter generation. In this design, an ARM11-based processor S3C6410 is used as the control system and the power supply uses a *low dropout regulator* (LDO) to minimize its noise impact on the signal.

The timing modulation circuit is used to generate a jittery clock signal as shown in Fig. 8. The required jitter is generated by controlling the LATCH of the delay line on the input clock signal. The control signal is divided into three signals so as to control the whole circuit. *Control_data [7:0]* controls the jitter profiles. When a single jitter control is performed, the jitter model in the ROM is called, and when the mixed jitter is performed, the data is written into the SRAM by the write address generator, read from the SRAM by the read address generator, and then it is sent to amplitude process. *Control_data [15:8]* configures the clock generator required for the amplitude process as well as the read and write address generator, ROM, and SRAM. *Control_data [23:16]* is used as the amplitude factor to calculate the magnitude of the delay and convert the final result into a 10-bit binary *D [9:0]* to control the delay line generating the jittery clock. *Analog_delay* is used to fine tune the delay line.

When using ROM as memory, this method can generate SJ, uniform jitter, BUJ, DCD and RJ. There are two examples of jitter generation design, one generates SJ and the other generates RJ. In order to generate SJ with a frequency of 10 MHz and an amplitude of 500 ps, we used 500 MHz to

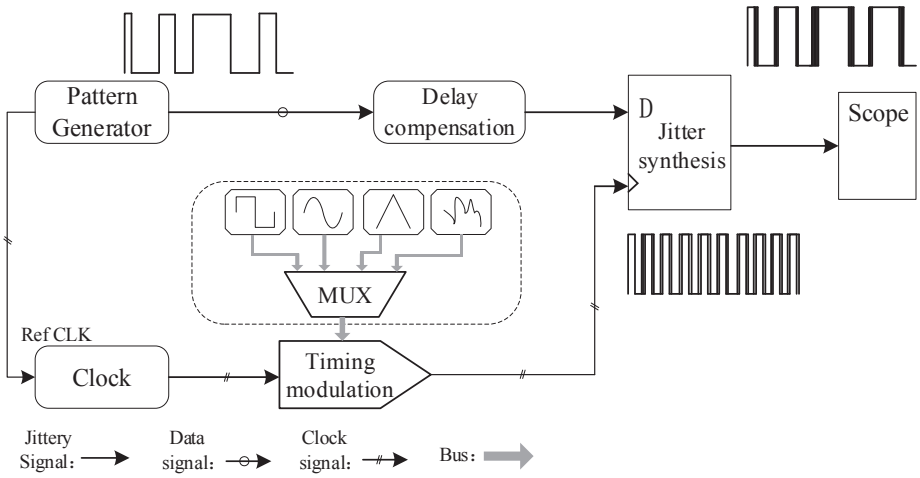


Fig. 7. The timing modulation method for jitter generation.

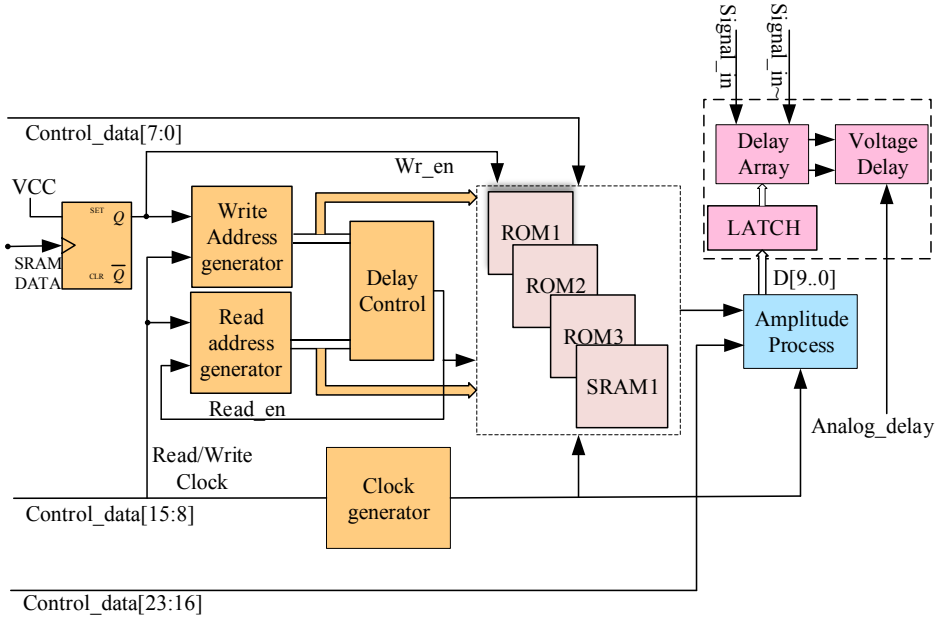


Fig. 8. Timing modulation circuit for generating controllable clock jitter.

generate 10 MHz jitter because SJ ROM has the capacity of 50 data and we applied the amplitude process of 2.5 to generate 500 ps jitter because the step of delay array is 10 picoseconds and the largest data in SJ is 200, as shown in Fig. 9. First, a 500 MHz clock is generated by the clock generator which is used to provide a clock for the read address generator to generate read addresses. Then the SJ data from ROM are read by read addresses where the data of SJ model are generated by (2) and are calculated in the amplitude process. Finally, control commands are sent to delay array to generate SJ. The timing diagram of generating an SJ is shown in Fig. 9.

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

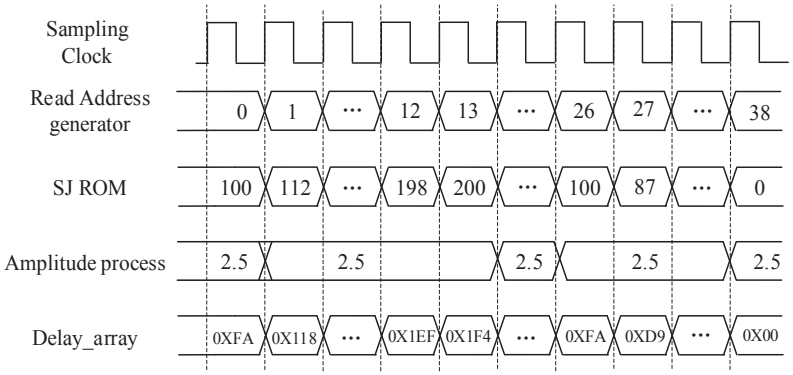


Fig. 9. Timing diagram of SJ generation.

The other example is generating RJ. In this paper, we can adjust σ of RJ as follows:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{N} (Fy_i - F\mu_0)^2}{N}} = F\sigma_0, \tag{9}$$

where σ_0 is original root mean square, μ_0 is original mean, y_i is data of RJ ROM, F is factor of the amplitude process, N is number of RJ ROM, and σ is root mean square of the generated RJ. In this paper, $\sigma_0 = 10$, and $\mu_0 = 0$. The process is similar to that of generating SJ as shown in Fig. 9 where SJ ROM is replaced with RJ ROM.

When using SRAM as memory, this method can generate jitter through superposition of SJ and DCD or superposition of SJ and SJ. There is a design example of generating mixed jitter. In order to generate mixed jitter with a frequency of 5 MHz and an amplitude of 3 ns, we used 250 MHz to generate 5 MHz jitter because mixed jitter SRAM has 50 data, and we applied the amplitude process of 1 to generate 3 ns jitter as the step of the delay array is 10 ps and the biggest number of data in SRAM is 300, as shown in Fig. 10. First, the host computer sends the command that that causes the generation of mixed jitter and calculates the data that needs to be stored in the SRAM. Next, the clock generator generates the clock and commands the write address generator to generate write addresses so the data are stored in the SRAM by write addresses. Then, the clock generated by the clock generator orders the read address generator to generate read addresses and the data in the SRAM are read by read addresses and sent to the amplitude process for calculation. Finally, control commands are sent to the delay array to generate mixed jitter. The timing diagram of generating mixed jitter is shown in Fig. 10.

Delay compensation is used to compensate for relative delay of the clock signal and the data signal. The delay compensation uses an MC100EP196 programmable delay line whose stepping is 10 ps. The resolution can set to 1ps by using fine control of voltage. The voltage control needs to use a high-precision DAC to provide correct voltage. According to actual debugging results, the delay accuracy decreases when the delay exceeds 8.333 ns [38].

As shown in Fig. 11, the schematic diagram of illustrates performing the jitter synthesis. The core action in the schematic diagram is jitter generation on the clock generated by the same clock of the data pattern. The high-precision digital PJ, DCD, BUJ, ISI and RJ models obtained by timing modulation are converted into quantitative jitter by the Delay Line to generate a jittery

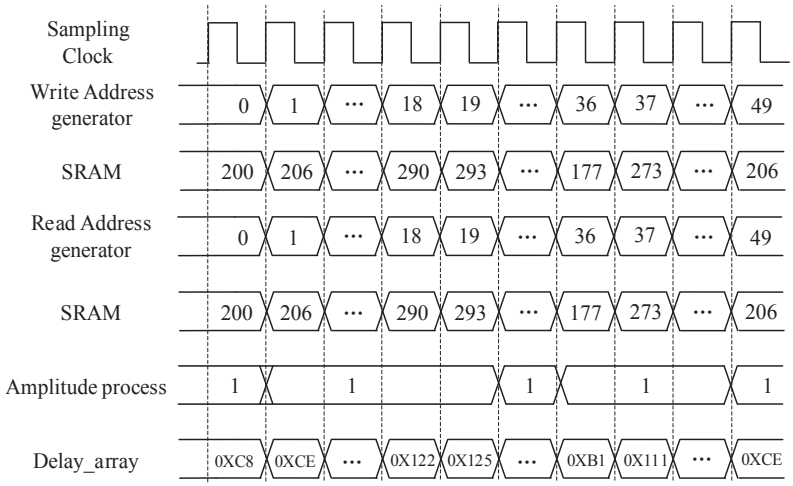


Fig. 10. Timing diagram of mixed jitter generation.

clock signal Finally the jittery data pattern is generated by D flip-flop where the data pattern generated by the pattern generator is connected to the D side of the D flip-flop, the jittery clock is connected to the CLK side of the D flip-flop, the Q side is the output of the jittery data pattern, and the D flip-flop output side Q is pulled to a low level or high level depending on the data pattern level when the rising edge of the jittery clock arrives. Thus, the jittery data pattern is synthesized because of the jittery clock [39].

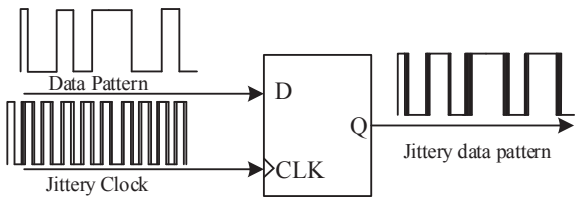


Fig. 11. Schematic of the principle of jitter synthesis [39].

5. Jitter measurement results

5.1. Comparing with analog modulation

The timing diagram of the system is shown in Fig. 12 depicting sinusoidal jitter generation where the same clock generates CLK and Pattern. Sinusoidal mapping is generated after the clock signal passes through the DTC. The output of the D flip-flop shows the result of the jitter generation.

The analog modulation method requires the cooperation of multiple instruments which is troublesome and uses the analog signal as a modulation signal. It directly introduces noise which is difficult to eliminate, affecting the effect of jitter generation.

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

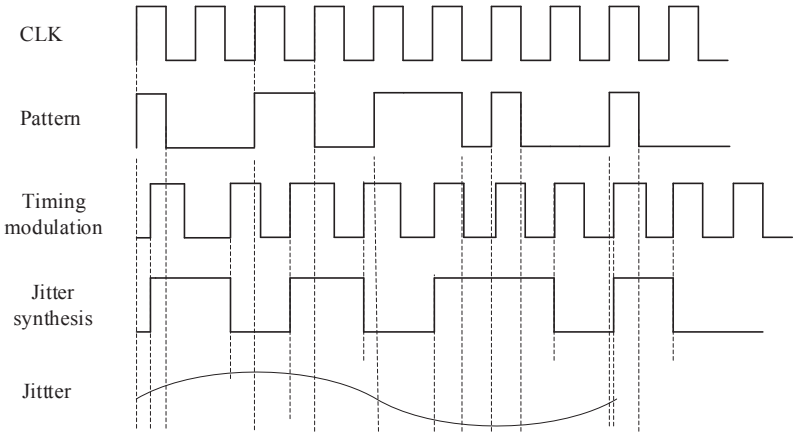


Fig. 12. The timing diagram of the system.

The magnitude of the jitter generated by analog modulation is: (in UI) [39]

$$A_{jitter} = \frac{\theta(t)_{p-p}}{2\pi} = \frac{D_f A_m}{\pi f_m}[UI_{p-p}], \tag{10}$$

where A_m is amplitude of the modulation signal, f_m is frequency of the modulation signal, D_f is frequency offset constant.

Analog modulation and timing modulation of this paper are compared in this paper as follows:

(1) According to Eq. (7), jitter amplitude is limited by D_f, f_m and A_m. If the jitter frequency increases, the jitter amplitude will decrease. However, the timing modulation method can adjust jitter frequency and jitter amplitude without limitation.

(2) Analog modulation requires the use of two signal sources and one pattern generator, while timing modulation method requires only one pattern generator and the module designed in this paper which greatly reduces the cost of the test.

(3) Analog modulation requires an analog signal which introduces undesired noise and affects the generated jitter. However, the timing modulation method uses all-digital synthesis to generate jitter and calibrates the generated jitter which greatly reduces the impact of noise.

(4) Analog modulation can only generate a single jitter signal and cannot generate DCD jitter. However, the method in this paper can generate single jitter and mixed jitter as well as can simulate various jitters, including periodic jitter and data dependent jitter.

5.2. Experimental test bench

To verify the accuracy and efficiency of jitter generation, we have designed and used an experimental test bench to measure the jitter components as shown in Fig. 13. An 81130A Agilent Pulse & Data generator was used to generate data pattern. An 813Zi-A LeCroy WaveMaster oscilloscope, with a bandwidth of 13G and a sampling rate of up to 40 GB/s was used to measure jitter. An N9010AAgilent EXA Signal Analyzer was used to measure DCD jitter frequency which has a frequency range from 10 Hz to 26.5 GHz. A clock module was used to obtain the clock of data pattern and a jitter module was used to generate jittery data pattern.

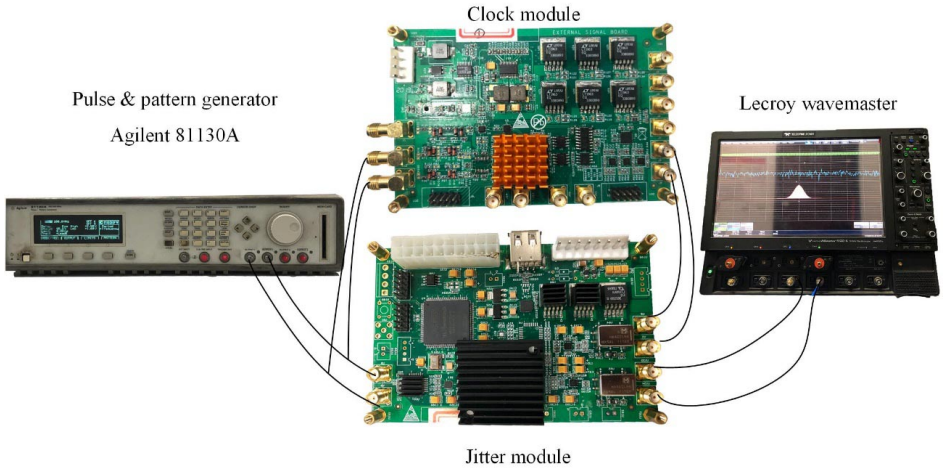


Fig. 13. Experimental test bench.

5.3. Validation of cross-point calibration

In the proposed cross-point calibration method, the accuracy of jitter generation is improved. As shown in Fig. 14(a), the eye cross is 36.14% before calibration and Fig. 14(b) shows the eye cross is 50.89% after calibration. It also can be seen that the DCD jitter is reduced from 31.114 ps to 321 fs. Moreover, the certain frequency components are attenuated in the spectrum as shown by the red circles in Fig. 14(c), 14(d). In this case, the ISI correction basically remains unchanged. Because the ISI is mainly derived from signal dispersion following the attenuation and reflection

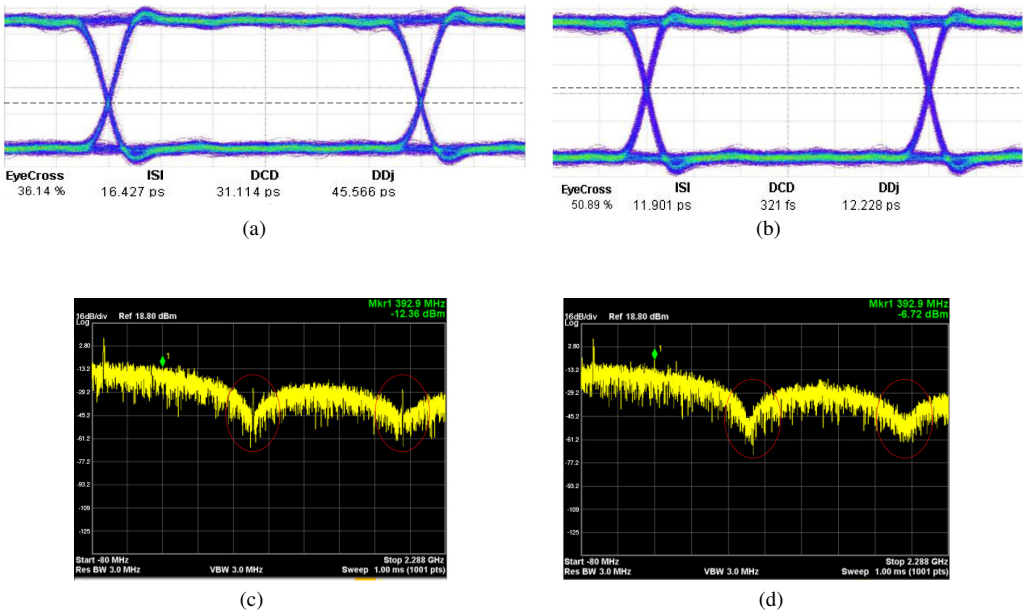


Fig. 14. Eye diagram and spectra for cross point calibration (a) the eye cross is 36.14% before calibration, (b) the eye cross is 50.89% after calibration, (c) Spectrum before calibration, (d) Spectrum after calibration.

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

of the transmission media [17–19], the cross-point position brings about the DCD, mainly due to the pulse width being changed relative to the nominal duty ratio of 50%. Therefore, this method can effectively improve accuracy of jitter generation.

This method can calibrate the cross point and improve accuracy by reducing the magnitude of unexpected DCD jitter. Moreover, the relative magnitude of the delay change and the cross-point position is shown in Fig. 15.

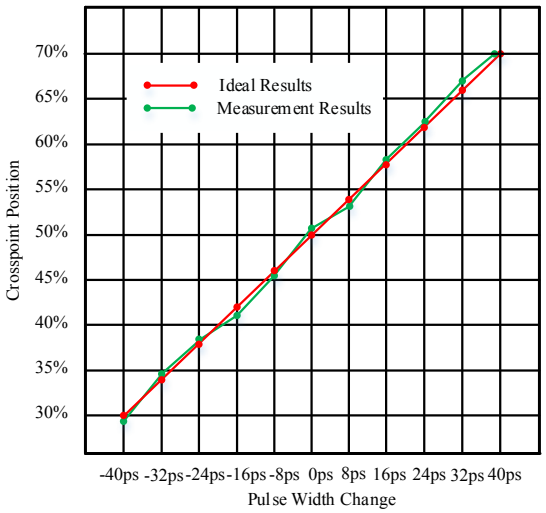


Fig. 15. Relative delay change vs. Cross-point position.

5.4. Comparison of the accuracy

The magnitude and frequency of jitter generation vary for jitter decomposition according to the Dual-Dirac model. In order to verify the accuracy of jitter generation, this paper compares the jitter generated by this method with the jitter method generated by analog modulation. As shown in Table 1, the jitter frequency resolution and amplitude resolution generated with this method are better than for analog modulation and this method can flexibly adjust jitter amplitude. To illustrate the benefit of the cross-point calibration, jitter amplitudes of PJ, BUJ, DCD, ISI and RJ are recorded with and without cross-point calibration as shown in Table 2 and Table 3. It can be seen that cross calibration makes the generated jitter close to the ideal value and improves the accuracy of jitter generation.

Table 1. Comparing jitter generation.

	[40]	[41]	**This paper with calibration**
Jitter frequency	1 Hz–100 MHz	1 kHz–20 MHz	1 Hz–20 MHz
Jitter frequency accuracy	±50 ppm	–	±20 ppm
Jitter amplitude	2.37 ns (32 Ui)	10 Ui	8.33 ns (28 Ui)
Jitter amplitude resolution	0.01 Ui (100 MHz)	0.01 Ui (20 MHz)	10 ps or 2 ps

Table 2. Amplitude of PJ and ISI with and without cross-point calibration.

Added jitter		**LeCroy Oscilloscope**			
		Without cross point calibration		**With cross point calibration**	
PJ (ns)	ISI (ns)	PJ (ns)	ISI (ns)	PJ (ns)	ISI (ns)
0.02	0.01	23.97 ps	19.77 ps	21.41 ps	14.02 ps
0.5	0.2	0.5234	0.2082	0.5174	0.2038
1	1.1	1.02	1.442	1.046	1.0476
2.284	4.1	2.284	4.116	2.2842	4.108
4.62	4.42	4.652	4.421	4.6226	4.419

Table 3. Amplitude of BUJ, DCD and RJ with and without cross-point calibration.

Added jitter			**LeCroy Oscilloscope**					
			Without cross point calibration			**With cross point calibration**		
BUJ (ns)	DCD (ns)	RJ (ns)	BUJ (ns)	DCD (ns)	RJ (ns)	BUJ (ns)	DCD (ns)	RJ (ns)
0.02	0.01	0.05	34.98 ps	14.77 ps	0.11	24.41 ps	13.18 ps	0.11
1.03	0.5	0.1	1.033	0.2084	0.19	1.032	0.2041	0.19
2.96	1.2	0.25	2.962	1.513	0.34	2.957	1.242	0.32
4.75	2.5	0.45	4.776	2.532	0.48	4.761	2.518	0.436
7.72	5	0.5	7.726	5.101	0.53	7.722	4.984	0.53

5.5. Validation of jitter generation

The jitter generation in this design is mainly based on the TIE jitter in the time domain model. Therefore, the test focuses on its TIE track and jitter is tested with an oscilloscope.

The histogram, TIE track, and the eye diagram of sinusoidal jitter are shown in Fig. 16 where the test signal frequency is 200 MHz, the jitter frequency is 999.3 Hz, the period jitter is

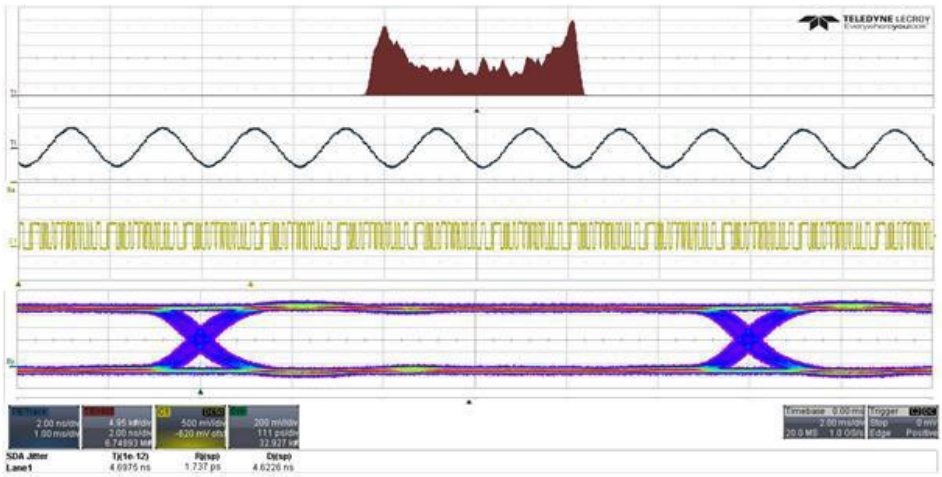


Fig. 16. Eye diagram, TIE track and histogram of sinusoidal jitter.

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

4.6226 ns (= 0.9245 UI) with cross-point calibration, the period jitter is 4.652 ns without cross-point calibration and the added jitter is 4.62 ns from the control system, and random jitter is 1.737 ps. The TIE track and histogram of random jitter is shown in Fig. 17 where the amplitude of random jitter is 436 ps with cross point calibration, RJ is 480 ps without cross point calibration and added RJ is 450 ps from the control system.

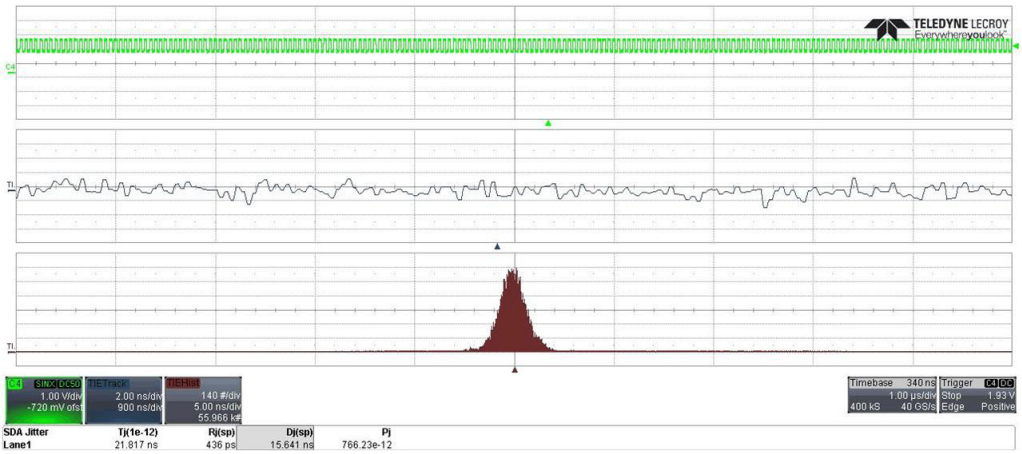


Fig. 17. TIE track and histogram of random jitter.

The eye diagram, TIE track, and the histogram of uniform jitter are shown in Fig. 18 where the test signal frequency is 200 MHz, the jitter frequency is 10.021 MHz, the BUJ is 24.41 ps (= 0.0049 UI) with-cross point calibration, the BUJ is 34.98 ps without cross-point calibration and the added jitter is 20 ps from the control system, and random jitter is 1.09 ps.

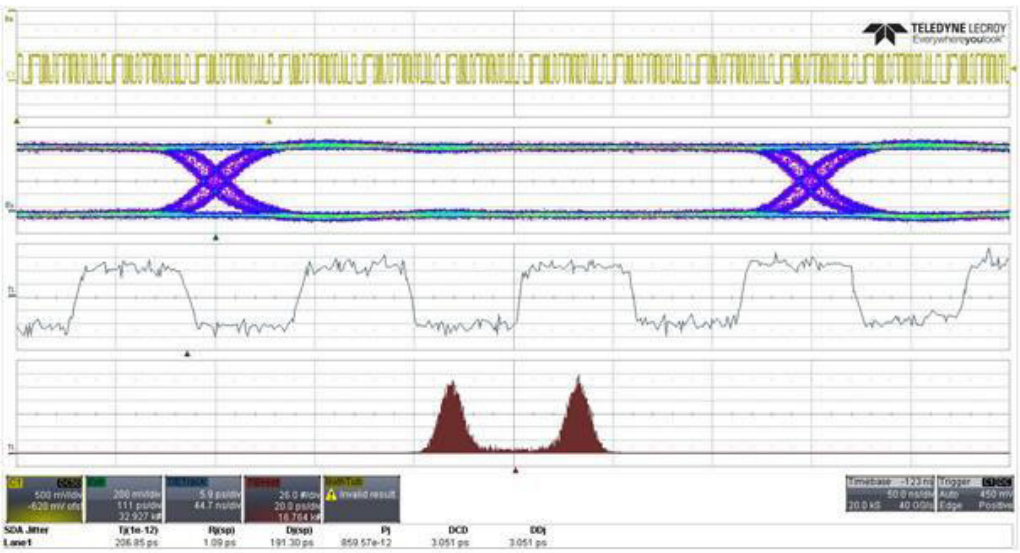


Fig. 18. Eye diagram, TIE track and histogram of rectangular jitter.

The TIE track and histogram of DCD jitter are shown in Fig. 19 where the test signal frequency is 400 MHz, the jitter frequency is 200 MHz, the DCD jitter is 1.242 ns with cross-point calibration, the DCD jitter is 1.513 ns without cross-point calibration, and the added DCD jitter is 1.2 ns from the control system.

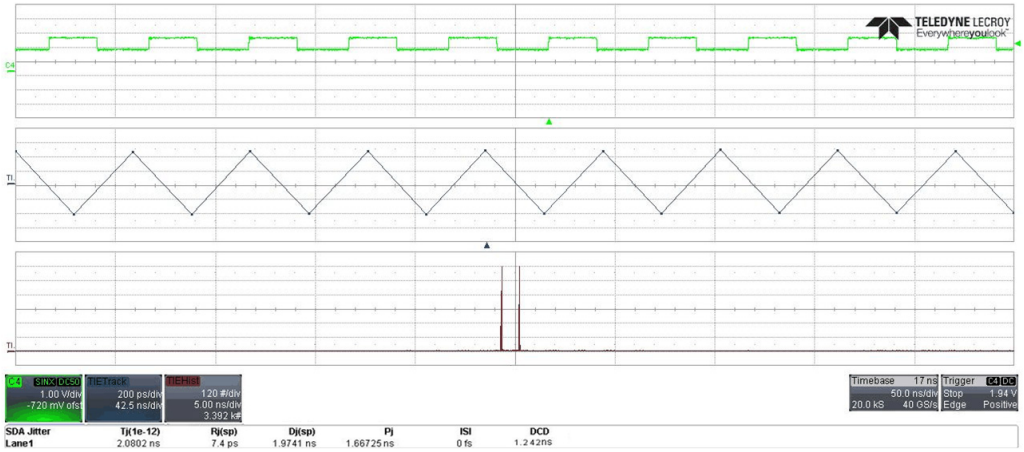


Fig. 19. TIE track and histogram of DCD.

The TIE track and histogram of *uniform jitter* (called ISI) are shown in Fig. 20 where the test signal frequency is 400 MHz, the jitter frequency is 252.3 Hz, the uniform jitter is 1.0476 ns with cross-point calibration, the uniform jitter is 1.442 ns without-cross point calibration, and the added uniform jitter is 1.1 ns from the control system.

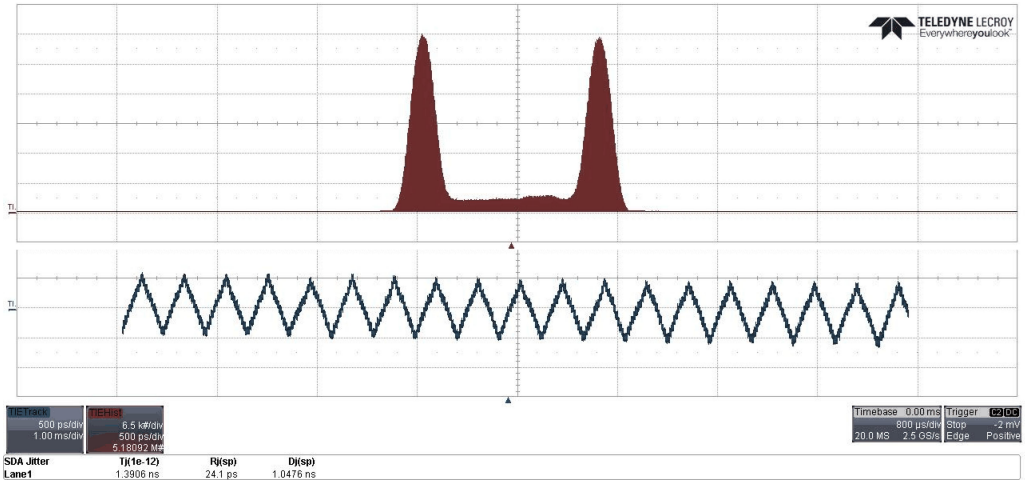


Fig. 20. Histogram and TIE track of triangular jitter.

The TIE tracks and corresponding jitter histograms are shown in Fig. 21 and Fig. 14, where the upper left corners are the simulated jitter histograms. Fig. 21 shows the simulation of the effect of DCD jitter and sinusoidal jitter on the data pattern and jitter models are from equation (2), (3),

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

(4), (5), (6), (7). Different frequencies, amplitudes, and phases of sinusoidal jitters are simulated as shown in Fig. 22. Therefore, they can also be seen as harmonics of different frequencies, amplitudes, and phases.

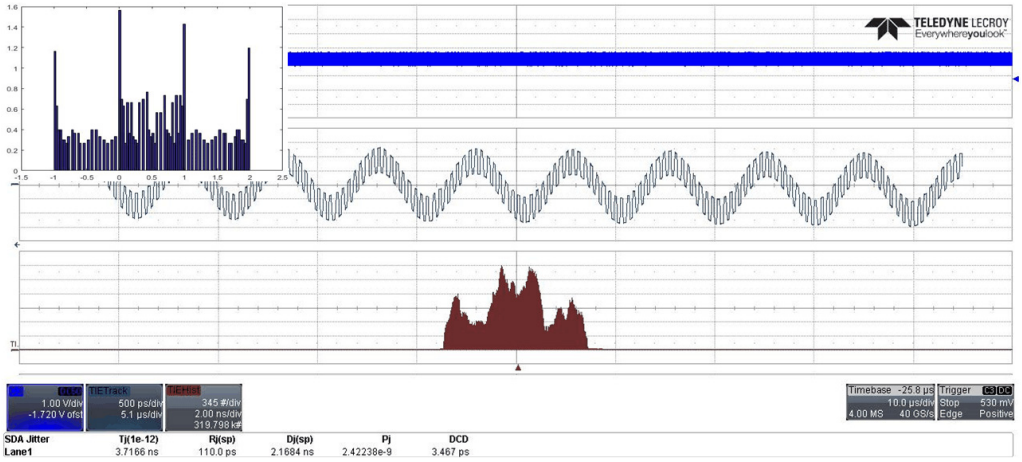


Fig. 21. TIE track and histogram of mixed jitter.

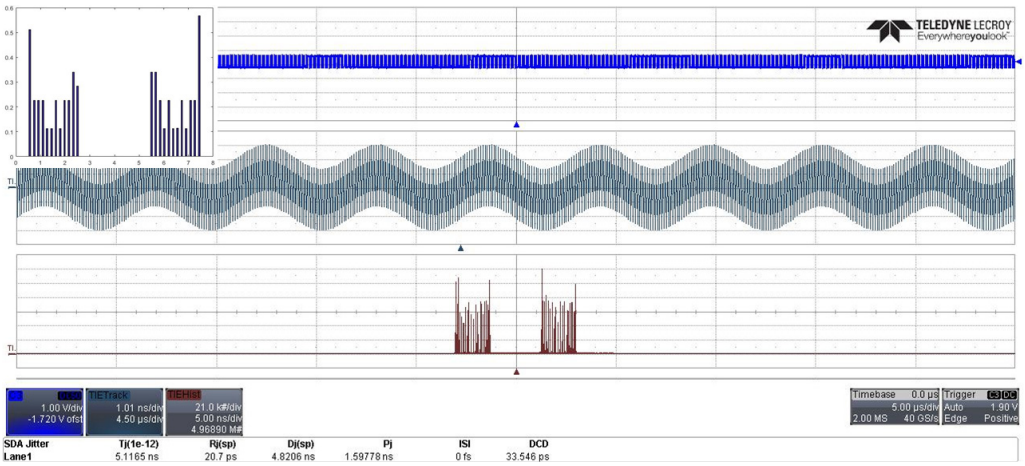


Fig. 22. TIE track and histogram of sinusoidal jitter of at different frequencies, amplitudes and phases.

6. Conclusions

In this paper, a new jitter generation technique using cross-point calibration and timing modulation for jitter decomposition is proposed. The generated jitter is pre-processed by cross-point calibration. This method improves the accuracy of jitter generation. It is equivalent to changing the pulse width to achieve compensation or attenuation of the cross point. The proposed timing modulation method realizes PJ, DCD, uniform and BUJ jitter, and mixed jitter which is equivalent to converting controllable digital delay to jitter. Comparing with the traditional method,

this method can freely control jitter frequency and amplitude, reduces the influence of noise and test cost, improves jitter accuracy, simulates the complex jitter that exists in actual circuits, and provides an experimental test bench for the jitter decomposition algorithm.

In future work, we prepare to verify and compare the accuracy of the existing jitter decomposition algorithm through the generated jitter with the method proposed in this paper.

References

[1] Sotiriadis, P. P. (2010). Theory of flying-adder frequency synthesizers – Part I: modeling, signals' periods and output average frequency. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *57*(5), 1935–1948. https://doi.org/10.1109/TCSI.2009.2039834

[2] Stephens, R. (2004). *Jitter analysis: The dual-Dirac model, RJ/DJ, and Q-scale*. [White Paper, v.1.0a]. https://www.keysight.com/upload/cmc_upload/All/dualdirac1.pdf

[3] Chada, A., Mutnury, B., Dikhaminjia, N., Tsiklauri, M., Fan, J., & Drewniak, J. L. (2018). Improved Transmitter Jitter Modeling for Accurate Bit Error Rate (BER) Eye Contours Using Transient Simulation of Short Bit Patterns. *IEEE Transactions on Electromagnetic Compatibility*, *60*(2), 1520–1528. https://doi.org/10.1109/TEMC.2017.2776080

[4] Tektronix. (2005). *Jitter Generation Techniques for Serializer-Deserializer Compliance Testing*. [Application Note]. https://m.eet.com/media-/1109453/tek_18568.pdf

[5] Li, M. P. (2007). *Jitter, noise, and signal integrity at high-speed*. Pearson Education.

[6] Da Dalt, N., & Sheikholeslami, A. (2018). *Understanding Jitter and Phase Noise: A Circuits and Systems Perspective*. Cambridge University Press.

[7] Duan, Y., Wu, H., Shimanouchi, M., Li, M. P., & Chen, D. (2018). A Low-Cost Comparator-Based Method for Accurate Decomposition of Deterministic Jitter in High-Speed Links. *IEEE Transactions on Electromagnetic Compatibility*, *61*(2), 521–531. https://doi.org/10.1109/TEMC.2018.2821680

[8] Mistry, D., Joshi, S., & Agrawal, N. (2015). A novel jitter separation method based on Gaussian mixture model. *Proceedings of 2015 International Conference on Pervasive Computing (ICPC)*. India. https://doi.org/10.1109/PERVASIVE.2015.7087091

[9] Dou, Q., & Abraham, J. A. (2006, March). Jitter decomposition by time lag correlation. *7th International Symposium on Quality Electronic Design (ISQED'06)*, USA. https://doi.org/10.1109/ISQED.2006.78

[10] Ku, C. K., Goay, C. H., Ahmad, N. S., & Goh, P. (2019). Jitter Decomposition of High-Speed Data Signals from Jitter Histograms with a Pole–Residue Representation Using Multilayer Perceptron Neural Networks. *IEEE Transactions on Electromagnetic Compatibility*, *62*(2), 2227–2237. https://doi.org/10.1109/TEMC.2019.2936000

[11] Soliman G. (2019). Improved Jitter Distribution Tail-Fitting Algorithm for Decomposition of Random and Deterministic Jitter. *IEEE Transactions on Electromagnetic Compatibility*, *62*(2), 1852–1857. https://doi.org/10.1109/TEMC.2019.2947222

[12] Nan, F., Wang, Y., Li, F., Yang, W., & Ma, X. (2009). A better method than tail-fitting algorithm for jitter separation based on Gaussian mixture model. *Journal of Electronic Testing*, *25*(3), 337. https://doi.org/10.1007/s10836-009-5112-8

[13] Pang, H., Zhu, J., & Huang, W. (2009). Jitter decomposition by fast Fourier transform and time lag correlation. In 2009 International Conference on Communications, Circuits and Systems, USA, 365–368. https://doi.org/10.1109/ICCCAS.2009.5250491

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

[14] Joseph, F., Hilliges, K. D., & Owen, C. L. (2007). *U.S. Patent No. 7,184,469*. Washington, DC: U.S. Patent and Trademark Office.

[15] Calvin, J. C., & Richmond, G. K. (2012). *U.S. Patent No. 8,224,613*. Washington, DC: U.S. Patent and Trademark Office.

[16] Desai, S. R., & Pickerd, J. J. (2014). *U.S. Patent No. 8,650,010*. Washington, DC: U.S. Patent and Trademark Office.

[17] Takauchi, H., Tamura, H., Matsubara, S., Kibune, M., Doi, Y., Chiba, T., Anbutsu, H., Yamaguchi, H., Mori, T, Takatsu, M., Gotoh, K., Sakai T., & Yamamura T., (2003). A CMOS Multichannel 10Gb/s Transceiver. *IEEE Journal of Solid-State Circuits*, *38*(12), 2094–2100. https://doi.org/10.1109/ISSCC.2003.1234212

[18] B. Ham. (2004). Fibre channel – Methodologies for jitter and signal quality specification -MJSQ, *Proceedings of InterNational Committee for Information Technology Standards (INCITS)*, 29–38.

[19] Tektronix. (2002). *Understanding and characterizing timing jitter* [Application note].

[20] Agilent. (2004). *Analyzing Digital Jitter and its Components* [Technical Note]. https://www.keysight.com/upload/cmc_upload/All/Analyzing_Digital_Jitter_and_its_Components.pdf

[21] Li, Y., Bielby, S., Chowdhury, A., & Roberts, G. W. (2016). A Jitter Injection Signal Generation and Extraction System for Embedded Test of High-Speed Data I/O. *Journal of Electronic Testing*, *32*(4), 423–436. https://doi.org/10.1109/IMS3TW.2015.7177879

[22] İspir, M., Özdil, Ö., & Yıldırım, A. (2013). Coloured noise generation with IFFT. *IET Intelligent Signal Processing Conference 2013 (ISP 2013)*. UK. https://doi.org/10.1049/cp.2013.2062

[23] Bidaj, K., Begueret, J. B., & Deroo, J. (2018). Jitter definition, measurement, generation, analysis, and decomposition. *International Journal of Circuit Theory and Applications*, *46*(12), 2171–2188. https://doi.org/10.1002/cta.2559

[24] Xia, T., Song, P., Jenkins, K. A., & Lo, J. C. (2004). Delay chain based programmable jitter generator. *Proceedings of Ninth IEEE European Test Symposium* (ETS 2004), France. https://doi.org/10.1109/ETSYM.2004.1347578

[25] Jovanovic, G., Stojcev, M., Nikolic, T., & Stamenkovic, Z. (2012). Programmable jitter generator based on voltage-controlled delay line. *Scientific Publications of the State University of Novi Pazar Series A: Applied Mathematics, Informatics and mechanics*, *4*(1), 61–73.

[26] Jovanović, G., Stojčev, M., & Nikolić, T. (2013). Clock jitter generator with picoseconds resolution. *International Journal of Electronics*, *100*(3), 779–792. https://doi.org/10.1080/00207217.2012.720953

[27] Calbaza, D. E., & Savaria, Y. (1999). Jitter model of direct digital synthesis clock generators. *IEEE International Symposium on Circuits and Systems (ISCAS),* USA. https://doi.org/10.1109/ISCAS.1999.777791

[28] Bidaj, K., Begueret, J. B., & Deroo, J. (2017). Generation of Colored Noise Patterns with Gaussian Jitter Distribution. *IEEE Transactions on Instrumentation and Measurement*, *66*(7), 2576–2584. https://doi.org/10.1109/TIM.2017.2711738

[29] Balestrieri, E., Picariello, F., Rapuano, S., & Tudosa, I. (2019). Review on jitter terminology and definitions. Measurement, *145*, 264–273. https://doi.org/10.1016/j.measurement.2019.05.047

[30] Cidon, I., Khamisy, A., & Sidi, M. (1994). Dispersed messages in discrete-time queues: delay, jitter and threshold crossing. *Proceedings of INFOCOM'94 Conference on Computer Communications*, Canada, 218–223. https://doi.org/10.1109/INFCOM.1994.337614

[31] Ameri, A., & Roberts, G. W. (2011). Time-mode reconstruction iir filters for ΣΔ phase modulation applications, Edition of the Great Lakes Symposium on VLSI. *Proceedings of the 21st edition of the Great Lakes symposium on VLSI*, Switzerland, 423–426. https://doi.org/10.1145/1973009.1973099

[32] Li, M., Peng, H. M., & Liao, C. S. (2000). Fast computation of time deviation and modified Allan deviation for telecommunications clock stability characterization. *Proceedings of International Symposium on Parallel Architectures, Algorithms and Networks. I-SPAN 2000*, USA, 156–160. https://doi.org/10.1109/ISPAN.2000.900280

[33] Schnecker, M. (2012). *Jitter Measurements in Serial Data Signals* [White paper]. LeCroy Corporation. http://cdn.teledynelecroy.com/files/whitepapers/wp_jittermeasurement_in_serialdatasignals.pdf

[34] Zamek, I., & Zamek, S. (2005). Definitions of jitter measurement terms and relationships. *IEEE International Conference on Test*, USA. https://doi.org/10.1109/TEST.2005.1583959

[35] Duan, Y., Wu, H., Shimanouchi, M., Li, M. P., & Chen, D. (2018). A Low-Cost Comparator-Based Method for Accurate Decomposition of Deterministic Jitter in High-Speed Links. *IEEE Transactions on Electromagnetic Compatibility*, *61*(2), 521–531. https://doi.org/10.1109/TEMC.2018.2821680

[36] Marcu, M., Durbha, S., & Gupta, S. (2008). Duty-cycle distortion and specifications for jitter test-signal generation. *Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, USA. https://doi.org/10.1109/ISEMC.2008.4652150

[37] Liang, T., Fu, Z., Liu, H., Liu, K., & Xiao, Y. (2019). Minimizing the Jitter of Duty Cycle Distortion Correction Technology Based on Cross Point Eye Diagram Correction. *IEEE Access*, *7*, 106238–106247. https://doi.org/10.1109/ACCESS.2019.2931474

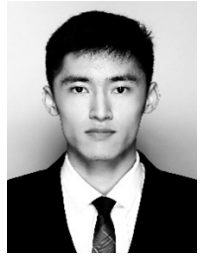
[38] Fu, Z., Liu, H., & Ren, N. (2018). Methodology for digital synthesis of ultra-narrow pulses. *Electronics Letters*, *54*(16), 969–970. https://doi.org/10.1049/el.2018.1218

[39] Ren, N., Fu, Z., Lei, S., Liu, H., & Tian, S. (2019). Methodology for Digital Synthesis of Deterministic and Random Jitter Generation on Rising or Falling Edges of Data Pattern. *Electronics, 8*(12), 1510–1525. https://doi.org/10.3390/electronics8121510

[40] Keysight Technologies. (2017). *Keysight N4963A Clock Synthesizer 13.5 GHz* [User's Guide]. http://literature.cdn.keysight.com/litweb/pdf/N4963-91021.pdf

[41] SHF Communication Technologies AG. (2017). *Creating Complex Jittered Test Patterns* [Application Note]. https://www.shfcommunication.com/wp-content/uploads/appnotes/shf_app_note_jitter_with_awg.pdf

Nan Ren was born in 1995. He is currently working toward the Ph.D. degree in instrument science and technology with the University of Electronic Science and Technology of China, Chengdu, China.
His research interests include instrument science and technology, circuits and system, automatic testing and system integration technology, jitter test and generating technology and so on.



Hanglin Liu received the B.S. and M.S. degrees in instrumentation engineering, in 2015 and 2018, respectively from the University of Electronic Science and Technology of China, (UESTC), Chengdu, China, where he is currently working toward the Ph.D. degree in instrument science and technology.
His main research interest is automatic digital testing technology and systems.

Metrol. Meas. Syst., Vol. 28 (2021), No. 1, pp. 123–143
DOI: 10.24425/mms.2021.135993

Zaiming Fu (Member, IEEE) was born in Sichuan Province, China, in 1977. He received the master's and Ph.D. degrees in test measurement and instrumentation from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2004 and 2010, respectively. He is currently a Professor with the School of Automation Engineering, UESTC. His research interests include data generator and pulse generator, measurement and instrument, signal processing, and so on.

Shengcun Lei was born in 1995. He is currently working toward the master's degree in instrumentation engineering with the University of Electronic Science and Technology of China, Chengdu, China. His research interests include instrument and meter engineering, circuits and system, automatic testing and jitter test, and generating technology.

Shulin Tian was born in Sichuan Province, China, in 1968. He received the M.S. and Ph.D. degrees in test measurement and instrumentation from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1991 and 2009, respectively.
He is currently a Professor with the School of Automation Engineering, UESTC. He has led a number of projects including high-speed, high-precision data acquisition, network and communication testing, testing bus technology, and testing system integration. His research interests include testability analysis and fault diagnosis of electronic device systems, and broadband time-domain testing technology and instrument.