METHODS OF PRECISE DETERMINING THE TRANSFER FUNCTION OF PICOSECOND TIME-TO-DIGITAL CONVERTERS

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Abstract

We present two main ways to precisely create the equivalent transfer function of picosecond time-to-digital converters based on commonly used method with tapped time coding delay lines. The ways consist either in evaluation of the quantization steps boundaries of the delay lines or in summation of numbers of the line quantization steps. The paper contains results of comprehensive analysis of both methods. The advantage and high versatility of the addition method is demonstrated.

Keywords: time-to-digital converter, equivalent conversion function, delay line, multi-edge coding, wave-union.

1. Introduction

Continuous research on increasing measurement resolution of precision time-to-digital (T/D) converters means that apart from the implementation of the converters in latest microelectronic technologies, innovative measurement methods are also still being sought. In the group of digital conversion methods, two of them are currently the most popular, namely the method based on simultaneous encoding of the measured time interval in independent *time coding delay lines* (TDLs) [1] and the method with propagation of multiedge rectangular signal in a single TDL, usually known as the wave union [2]. Both methods mentioned above originate from the previously developed solution in which a measured time interval is encoded by measuring the propagation time of a single signal edge in a single TDL [3]. Measurement results obtained in both methods do not directly represent the value of the measured time interval and require appropriate calculations, adequate to the method used. In both cases it is necessary to create an equivalent transfer function which would enable the calculation of correct measurement results.

The remainder of this paper is organized as follows. The next two sections are devoted to a brief presentation of both analysed conversion methods, *i.e.*, first one based on encoding of

the measured time interval in independent TDLs (Section 2) and the other one consisting in the multiedge signal propagation in a single TDL (Section 3). Along with descriptions of the conversion methods, the Sections 2 and 3 explain how to create adequate transfer functions using, respectively, evaluation of the quantization steps boundaries of the delay lines and summation of numbers of the line quantization steps. Then, the use of number summation method in the converter with independent TDLs is described and comparison of both ways of transfer function creation is presented (Section 4). Next, the influence of timing jitter of quantization step boundaries on equivalent quantization steps widths is discussed (Section 5). Finally, results of analysis performed are discussed in conclusions (Section 6).

2. Method of independent delay lines with single edge signal propagation

The measurement system, based on the method of independent TDLs [1], consists of several TDLs, in which the edge of measured signal (usually the rising edge) is propagated and coded. The start of propagation is initialized simultaneously in all TDLs together with the beginning of measured time interval (T_m). At the end of T_m, the current logic states of delay cells in the TDLs are saved into the related parallel registers. The number of the last flip-flop in the register, reached by the propagating edge, represents the duration of T_m. The schematic diagram for example two TDLs has been presented in Fig. 1.
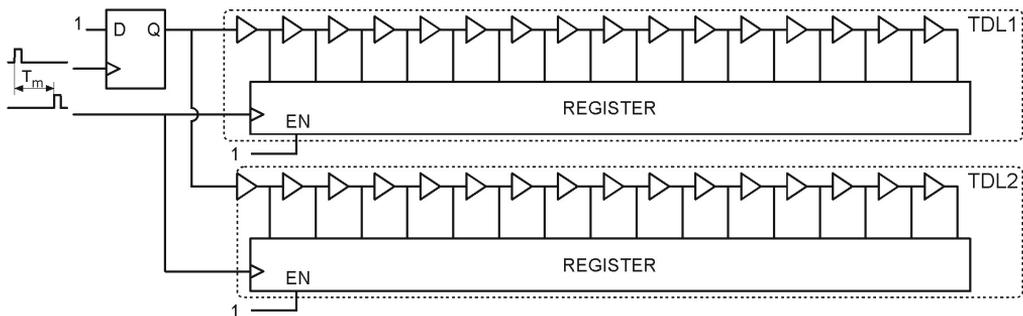

Fig. 1. Time-to-digital converter with two independent time coding delay lines.

Technological dispersion and heterogeneity of the structure of a CMOS integrated circuit cause edges of quantization steps in both lines (TDL1 and TDL2) to not overlap. Such a property makes it possible to increase the resolution. Due to mutual shifts of the quantization steps the creation of shorter virtual quantization steps is possible as shown in Fig. 2.
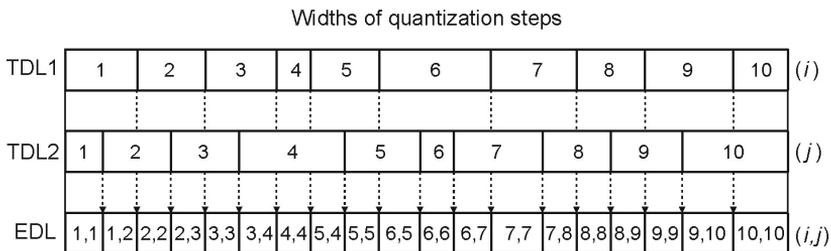

Fig. 2. Method for creating equivalent quantization steps for two independent time coding delay lines.

In order to determine an equivalent transfer function of the T/D converter, several operations should be carried out consecutively. First, the widths of quantization steps for each independent TDL should be evaluated [4–8]. Then quantization steps for the *equivalent time coding delay line* (EDL) representing both parallel TDLs (TDL1 and TDL2) are determined. This is achieved as follows. Let us assume that widths of quantization steps in TDL1 are named $QS1_k$, where $1 \leq k \leq m$ and m is steps number of TDL1, while in TDL2 are named $QS2_l$, where $1 \leq l \leq n$ and n is step number of TDL2, then the boundaries of consecutive quantization steps can be expressed for TDL1 and TDL2 as follows, respectively:

$$Q1e(i) = \sum_{k=1}^{i} QS1_k, \tag{1}$$

$$Q2e(j) = \sum_{l=1}^{j} QS2_l. \tag{2}$$

The EDL contains finally $n+m-$ quantization steps, and the durations of which are given by the following equation:

$$QE(i, j) = p\,Q1e(i) + (1 - p)Q2e(j), \tag{3}$$

where p is a predicate which takes values of zero or one, according to the relation:

$$p = \left(\sum_{k=1}^{i} QS1_k \leq \sum_{l=1}^{j} QS2_l \right). \tag{4}$$

This means that the predicate p for the quantization step (i, j) is equal to one, if the sum of i steps width of the first TDL is not larger than the sum of j steps width of the second TDL. Otherwise, the predicate p equals zero. The beginnings and ends of equivalent quantization steps are determined by the above boundaries of quantization steps, hence the width of individual quantization step can be presented as follows:

$$QSE_{i,j} = \begin{cases} QE(i, j) - QE(i - 1, j) & \text{for } QE(i - 1, j) > QE(i, j - 1) \\ QE(i, j) - QE(i, j - 1) & \text{for } QE(i - 1, j) < QE(i, j - 1) \end{cases}. \tag{5}$$

Determining the measurement result also requires the knowledge of the boundaries of quantization steps of each TDL in order to calculate the centre of an equivalent quantization step. However, it is calculated as the arithmetic average of boundaries of EDL quantization steps.

3. Method of multiedge signal propagation in a single time coding delay line

The measurement method, based on encoding of the multiedge signal [2], consists in propagation of a fixed digital standard signal, containing a finite number of states 0 and 1, in a single TDL. The schematic diagram of such a T/D converter is presented in Fig. 3. The pattern register contains a serial combination of logical states forming the so-called pattern, *e.g.* 01110001110. When the measurement is started, the pattern propagation in the line is triggered. The end of measurement causes the entry of TDL state into the register. The measurement result is determined on the basis of the numbers of consecutive flip-flops which registered changes in the pattern logical state 0–1 or 1–0. Increased resolution is obtained as a result of registering several logical state changes in the line, instead of a single state change, as in the classical method based on a single TDL [2].
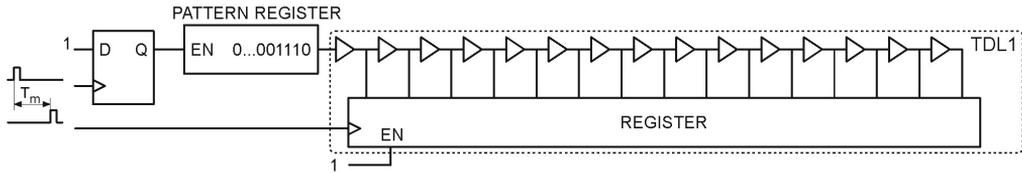
Fig. 3. T/D converter based on multiedge signal propagation in a single time coding delay line.

During the calibration process, based on the statistical code density test [4], random input events are counted for each quantization step of an EDL. Each step is given a number based on the sum of locations of flip-flops in registers which that changed their output states as a result of pattern propagation. In such a way, an equivalent transfer function of the EDL is directly obtained. There is no need to create separate functions for each active signal edge (*e.g.* the rising edge) in the pattern, and then compose them as in the method of independent TDLs described in section 2. An example of creating quantization steps of an EDL for two active edges is shown in Fig. 4.
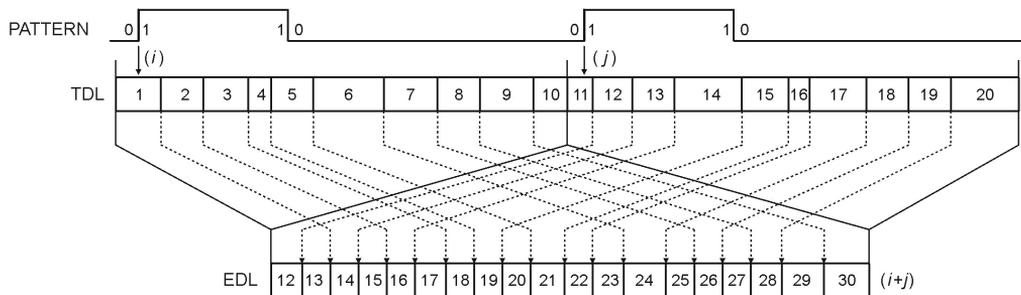

Fig. 4. Method of creating equivalent quantization steps for the converter with multiedge signal.

Thanks to this solution, during the calibration process the information on the widths of quantization steps of the EDL is obtained immediately. Moreover, a pattern should be selected so that each active edge changes only one quantization step during propagation in a TDL. In other words, the time interval between the edges should be large enough to counteract the overlap of the edges. Then the sum of locations of pattern active edges changes by one, and the boundaries of EDL quantization steps can be described by the relation:

$$QE(i, j) = \frac{N_i + N_j}{N},$$
(6)

where N_i and N_j are the numbers of events recorded by the flip-flop i and j, respectively for the first and second signal edge. Number N is the sum of all events recorded during the calibration process. The higher the number N, the more precisely the boundaries of quantization steps are defined [4, 7, 9, 10].

Theoretically, any number and combination of active edges can be used. However, it is necessary to bear in mind that differences in the propagation times of rising and falling slopes may cause pulse shrinking, which in long lines can ultimately lead to the disappearance of pulses.

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4. The use of number summation method in the converter with independent coding lines

The unusual simplicity of determining the equivalent function in the method [2] encouraged to try using it also in T/D converters with independent TDLs [1]. For this purpose, in order to compare it with the results obtained in [2], the research on a T/D converter with three independent TDLs was undertaken. A development kit with an FPGA (*Field Programmable Gate Array*) device of the Spartan-6 series (XC6SLX75-FGG484, Xilinx) was applied, in which a complete time counter operating according to Nutt's interpolation method was implemented [3]. A simplified block diagram of the interpolation time counter has been shown in Fig. 5.
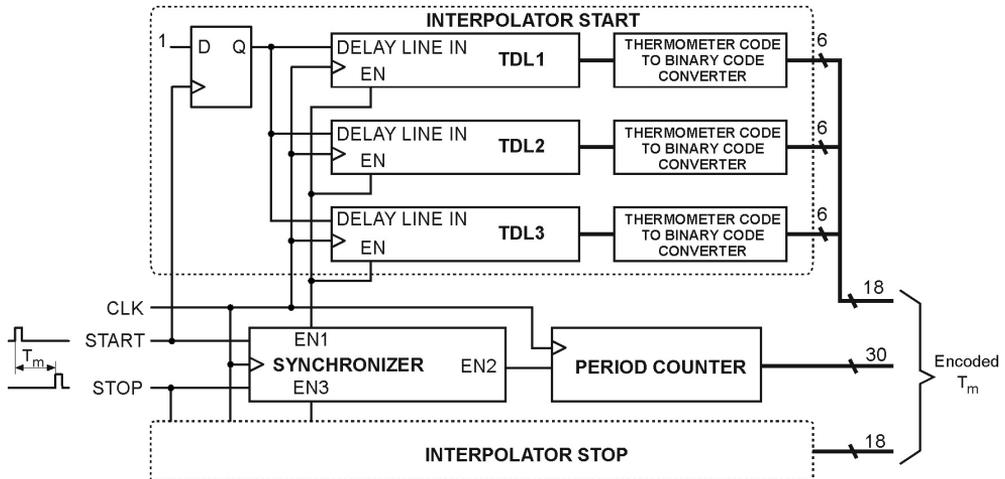

Fig. 5. Simplified block diagram of the interpolation time counter.

The first studies were aimed at identification of the quantization steps of individual interpolators in the START and STOP channels. The widths of steps of each TDL for the START channel have been presented in Fig. 6.
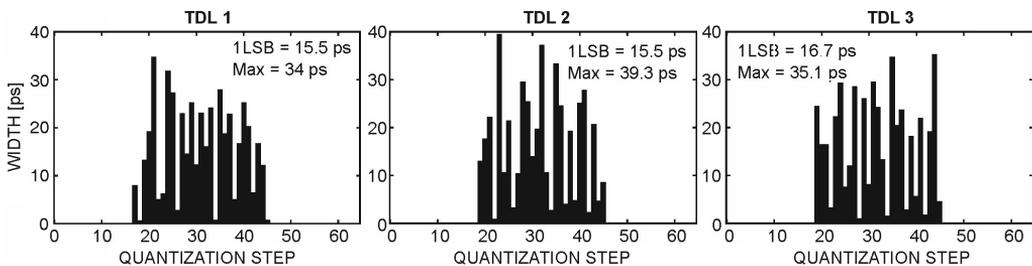

Fig. 6. Widths of the quantification steps for three time coding delay lines of a T/D converter.

Due to lack of possibility of precise control of connection paths delays in the FPGA device, the edge of pulse determining the beginning of measured time interval does not reach all TDLs at the same time. As a result, the active processing range of each line starts from a different number of the flip-flop (in TDL1 from the number 17 and in TDL2 and TDL3 from the number 19, see in Fig. 6). The average width of steps within the processing range of the TDL is about 16 ps. In the

next study, using the two above mentioned methods of EDL formation on the basis of data from the previous study, the widths of equivalent quantization steps were determined. They are shown in Fig. 7.
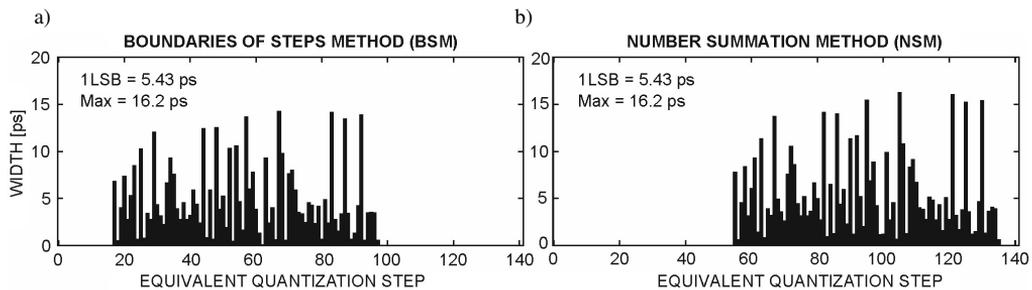

Fig. 7. Widths of ECL quantization steps determined by the two tested methods: boundaries of steps (a) and number summation (b).

In both cases (Figs 17a and 17b), the values of average and maximum width of steps are the same. In order to exactly check the differences between the determined widths of steps, it is necessary to renumber the quantization steps in such a way as to give the same number to the first quantization steps determined by both methods. Then in relation to the number summation method, differences in widths between equivalent quantization steps determined by both methods are shown in Fig. 8.
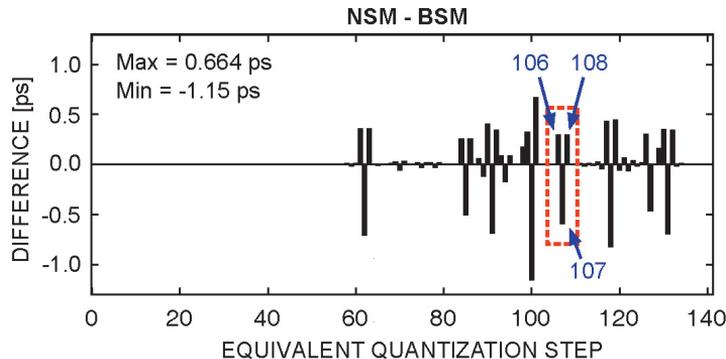

Fig. 8. Differences in the widths of equivalent quantization steps determined in both studied methods.

The obtained differences do not exceed 1 ps. From a theoretical point of view, both methods of determining the widths of equivalent quantization steps should give the same result. Existing differences may result, among others, from the timing jitter of pulse edges that influences the measured time interval, the metastability effect of flip-flops or other disturbances that cause non-simultaneous latching of parallel register flip-flops [11].

Another comparison of both methods for creating equivalent transfer functions comes from using them in the time interval conversion process. An example of 50 ns time interval, used for the test, was generated with the aid of a precision delay generator GFT1004 (*Greenfield Tech.*). The obtained histograms of 2000 measurement results are shown in Fig. 9. Distributions of measurement results are very similar and they have the same averages and standard deviations.
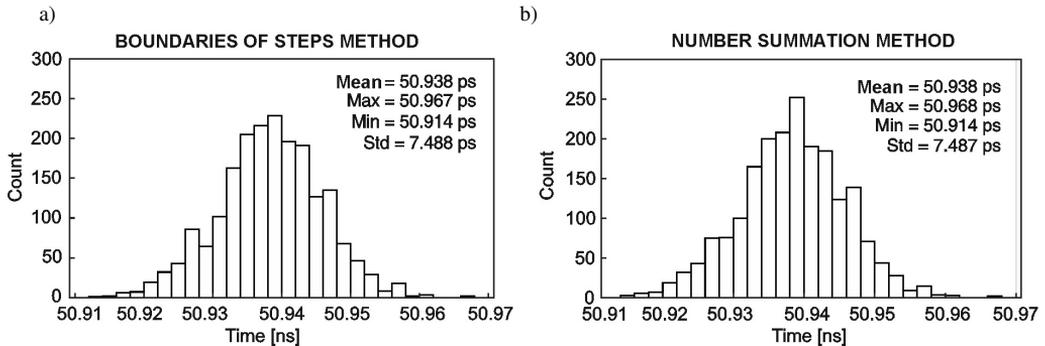
Fig. 9. Distributions of measurement results of an exemplary time interval obtained by means of equivalent transfer functions determined using the methods based consecutively on: evaluation of the quantization steps boundaries (a) and summation of quantization steps indexes (b).

5. Discussion

During the performed tests main metrological parameters were evaluated. One of them is the mean value of converter resolution, which is a numerical representation of the average quantization step (LSB). Both methods allow to obtain the same value of mean resolution despite the differences in widths of some particular equivalent steps of transfer functions. For example, the steps 106, 107 and 108 (Fig. 8) were considered because their adjacent steps do not introduce any differences in widths. Table 1 contains for each of the quantization step: the flip-flop number registered during the process of statistical calibration (flip-flops in parallel registers), equivalent quantization step widths achieved for both analysed methods and the percentage share of a given combination of flip-flop numbers in creating the number of an equivalent quantization step.

Table 1. Parameters of equivalent quantization steps: 106, 107 and 108, evaluated for both methods involved.

Equivalent step number in ECL	Equivalent step width (quant. steps boundaries)	Equivalent step width (number summation)	Combinations of TDLs step numbers			Measurement percentage of calibration
			Step number in DL1	Step number in DL2	Step number in DL3	
106	11.101 ps	10.806 ps	35	35	36	100 %
107	0.636 ps	1.226 ps	36	35	36	76%
			35	36	36	24%
108	8.626 ps	8.331 ps	36	36	36	100%

The influence of timing jitter of quantization step edges on equivalent quantization steps is clearly observed for narrow quantization channels (for example 107 in Fig. 10). Potential random changes of this narrow quantization step result from the influence of uncertainty of measured signal edges and random spread of propagation times of delay elements of TDLs [5, 11–13]. On the basis of values obtained during the calibration process and presented in Table 1, it is possible to observe a mutual change in the position of boundaries between steps 35 and 36 for lines DL1 and DL2 because the registration order of types 36–35 and 35–36 is changed, while for the third line DL3 one channel with number 36 is always active.
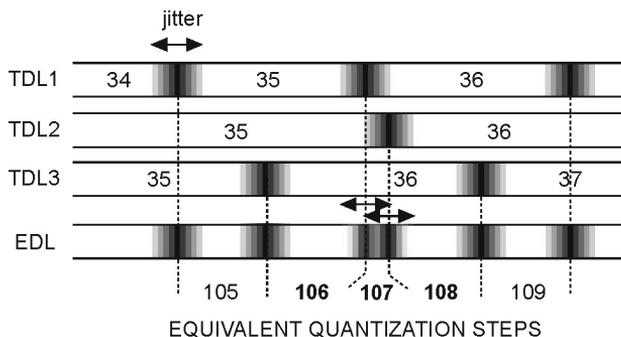
Fig. 10. Illustration of the influence of timing jitter phenomenon of the boundaries
of quantization steps on equivalent quantization steps widths.

This phenomenon is registered differently with the use of both tested methods. In the method based on evaluation of the quantization steps boundaries [1] such event is included in channels 106 or 108, respectively for events 35–36 and 36–35. The same situation for the number summation method [2] causes that the event is included in channel 107, because the number is created on the basis of sum 35 and 36, regardless of the mutual location of boundaries steps 35 and 36 in both lines TDL1 and TDL2. Therefore, comparing both methods for determining equivalent transfer functions for the analysed situation, channels 106 and 108 for the boundaries of quantization steps method will be wider than for the number summation method. However, step 107 for the second method is wider in comparison to the first method because the mutual exchange of boundaries of steps 35 and 36 is still recorded within the range of equivalent step 107. It causes the occurrence of a phenomenon which can be called the effect of masking the timing jitter of quantization boundaries and may have a positive influence on the measurement quality of a constant time interval measured with an interpolating time counter. This is observable for the results presented in Fig. 9. Comparing the measurement results of a constant time interval, it can be stated that the use of direct determination of equivalent quantization steps [2] can be applied to T/D converters with independent parallel time coding TDLs.

The timing jitter of quantization boundaries cannot be completely eliminated but it can be reduced by stabilization of measurement conditions. While temperature stability is usually provided using a climatic chamber, it is much more difficult to ensure a constant and filtered supply voltage. For T/D converters implemented in ASIC (*Application Specific Integrated Circuit*) devices, this problem is solved through the use of well-known integrated DLLs (*Delay-Locked Loops*). The DLL technique for the use with FPGA-based T/D converters is presented in [13].

However, it should be noted that the observed timing jitter of quantization boundaries provides important information about quality of the T/D conversion process. It can also be used to characterise the rank of integrated circuits in terms of the jitter introduced into processed signals. The smaller the differences between the widths of quantization step determined by the discussed methods, the smaller the jitter of the propagation time of TDLs elements (Fig. 8).

Due to the influence of external factors on the T/D converter, such as supply voltage, ambient temperature or electromagnetic radiation, the width of quantization steps can change. When this occurs after the quantization steps identification process, the conversion result will be calculated based on outdated transfer functions. Obviously, this will increase the measurement error. However, when the conversion result is calculated by the quantization boundaries method, it is possible to detect this error. After changing the quantization step boundaries, some flip-flop number com-

binations (i, j) which did not occur during the quantization steps identification process can be recorded. The occurrence of new combinations and the jitter of boundaries of quantization steps make it impossible to precisely determine the measurement result using the limits method. Since the equivalent coding line (3) does not contain the quantization steps $QE(i, j)$ indicated by the registered flip-flop number combinations (i, j), then it is necessary to average the results from each TDL separately *e.g.* $[Q1e(i) + Q2e(j)]/2$.

To confirm the assumption above, experimental studies were performed, where quantization steps of the converter at an ambient temperature of 25°C were identified as a reference. Then ambient temperature was changed successively within range from 0°C to 50°C, and 2000 measurements of the 50 ns time interval were carried out. During the measurements, the number of incorrect combinations of flip-flops numbers (i, j) was recorded. The results of the study are presented in Table 2.

Table 2. The dependence of the number of new flip-flops combinations and measurement uncertainty on the ambient temperature.

Temperature [°C]	0	10	**25**	40	50
Number of incorrect flip-flops combinations	644	463	**114**	284	529
Measurement uncertainty [ps]	27.0	17.2	**7.5**	16.8	31.5

As expected, an increase in the ambient temperature leads to an increase in the number of incorrect flip-flop combinations. Thus, the measurement precision deteriorates. The observed dependence gives the basis for considering the number of incorrect flip-flops combinations as a reliable indicator of the time counter decalibration. It might seem that the standard deviation of results of the time interval measurement is a good indicator of the time counter decalibration. However, the standard deviation is not an optimal indicator because its value depends both on the quality of counter calibration and the quality of the source of the measured time interval. If for some reasons the source starts generating time intervals imprecisely, the deviation of the measurement results will increase, and the reason for this increase will be the source of the time interval, not the counter. The number of incorrect flip-flop combinations changes only when the propagation time of the elements used for the TDL construction changes. Therefore, its continuous monitoring will allow to assess the counter's measurement performance.

6. Conclusions

The performed research on determining the equivalent transfer functions of T/D converters using two methods based consecutively on (1) evaluation of the quantization steps boundaries of the time coding delay lines and (2) summation of numbers of the lines' quantization steps, has led to the following conclusions and observations. Due to inherent converter timing jitter and various algorithms for evaluation of equivalent transfer functions in both methods the differences in widths of quantization steps of transfer functions obtained with the use of these methods are observed. However, the revealed differences do not influence the mean value of converter resolution, which is exactly the same for both tested methods (5.43 ps). Also, the precision of serial measurements is the same in both cases (7.49 ps for an exemplary measurement). Identified minor differences in transfer functions can be of importance only in the case of a single measurement when hitting a particular quantization step determines the measurement result, but during typical serial measurements the influence of jitter of quantization steps edges is averaged out.

In view of comparable metrological properties of both methods, the design conclusion becomes significant. The method of numbers summation, proposed in [2], is simpler in terms of computational complexity and enables to directly obtain equivalent transfer function using results of calibration based on the method of statistical identifications, *e.g.*, easily executed statistical code density test. Moreover, it allows for a simple implementation in an FPGA device, thanks to the use of built-in memory for storing calibration results, *i.e.*, the values of equivalent widths of steps involved in the measurement result determination.

Acknowledgements

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