

# Study of Capacitor & Diode Aging effects on Output Ripple in Voltage Regulators and Prognostic Detection of Failure

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**Abstract— Objectives:** To design and simulate a buck converter and detector circuit which can prognostically indicate the power supply failure. Failure of Aluminium Electrolytic Capacitor (AEC) is considered as the parameter causing the power supply failure. To analyse variation of output ripple voltage due to possible changes in the Equivalent Series Resistance (ESR) and effective capacitance of the capacitor and design a detector to detect the failure of power supply prognostically.

**Methods:** A DC-DC buck converter in SMPS topology is designed by assuming an input voltage of 12V with 3 volts possible fluctuations and an output voltage of 3.3 volts is desired. Simulation is carried out to measure the variation in output ripple voltage caused due to aging of electrolytic capacitor using TINA by Texas Instruments. A detector is also designed to compare the ripple voltage and a predefined threshold voltage so as to indicate the possible failure of Switched Mode Power Supply (SMPS) well in advance by monitoring the output ripple increase.

**Novelty:** Having a fault tolerant power supply is very important in safety critical applications. Here by monitoring the output ripple variation, the degradation of AEC is predicted by calculating the ESR and capacitance variation. This simple yet effective prognostic detection will support in the design of fault tolerant power supplies.

**Highlight:** It is found that, the ripple at the output increases with aging of the electrolytic capacitor, as with time the equivalent capacitance decreases and Equivalent Series Resistance (ESR) of the capacitor increases. The designed detector output is found to prognostically indicate the failure of SMPS.

**Keywords—**Buck; MOSFET; ESR; SMPS; voltage ripple

## I. INTRODUCTION

MODERN electronic Devices need to feed internally different sub circuits whose purpose and specifications are widely different from one another. Some of these sub circuit blocks require voltages from 3.3V to 5V and in the case of ultra-low power applications they need voltages of 0.5V [1]. To satisfy these requirements Power Management Units (PMU) are used as interface between main power supply and sub circuits which provide those required voltages by using power converters [1, 2, 3]. Fig. 1 depicts how a PMU interfaces sub-circuits in a system. Switching regulators form basic building block of power management Units which use either a buck or boost converter. A DC regulator can have different topologies, of which most commonly used and efficient is a Switched Mode Power Supply (SMPS). Semiconductor devices are extensively used in SMPS design. A MOSFET switch, buck converter and

a capacitor are the major components in SMPS design. Fig.2 indicates basic buck topology. Among available three types of capacitors, Aluminium Capacitors are the most popular type of capacitor used in the power converter systems due to its low cost and high energy density.

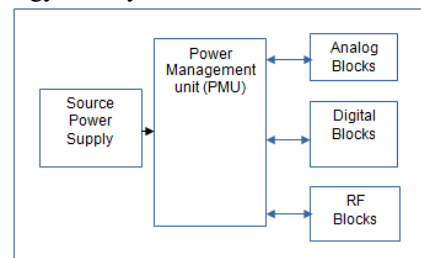


Fig.1. PMU Powering Sub-Circuits

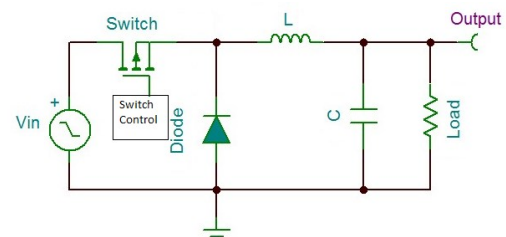


Fig.2. Buck Converter with Freewheeling Diode

It is observed that components used in power supplies are susceptible to failure mainly due to reasons like -changing atmospheric conditions, current and voltage transients, modelling and manufacturing faults, overload, short circuit, breaking of track, aging etc. [4]. Also, few of the failures are random for which the reasons are unknown. An industry-based survey was carried out with various automotive and aerospace electrical drives and power converter users, which concluded that power semiconductors are the most prone to failure (31%), followed by capacitors (17%) [4]. However, about 30% of power electronic system failure is due to capacitor failure. This demands for the need to have a simple method to identify the SMPS failure due to the failure of AEC. When a component fails, fluctuations in voltage and/or current levels may occur at different parts of the power supply circuit. This might also result in the abnormal behaviour of components or even in the shutdown of the converter. In safety critical applications, such power supply failure may lead to fatal consequences. Most power converters use Aluminium-Capacitors and the variation

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of its ESR is the most used health indicator for these Capacitors. Both effective capacitance and ESR indicates the health status of a capacitor and estimations combining the capacitance and ESR provides greater accuracy.

TABLE I  
FAILURE RATE CONTRIBUTION BY DIFFERENT COMPONENTS TO SMPS FAILURE

Components Contributing to Power Supply Failure	% of Failure
Power Semiconductors	31
Capacitors	17
Gate Drives	15
Connectors	12
Inductors	5
Resistors	2

Health monitoring techniques are mainly of 2 types: Online and offline. Online health monitoring techniques are employed often than offline techniques. However, the degradation of capacitor is generally slow and thus offline techniques also offer greater accuracy and are also simple in monitoring the health of capacitors. When a health monitoring technique is proposed requirement to additional hardware, cost, volume is kept in check. Also, accuracy, scalability, maintainability, reliability, adaptability are important factors in considering a health monitoring algorithm.

## II. BACKGROUND

Aluminum electrolytic capacitors are substantially used in design of Switched Mode Power Supply due to their large capacitance and low cost [1,4]. However, they have high failure rate contributing to major part of SMPS failure. Physical structure of an Aluminium Electrolytic Capacitor is illustrated in fig. 3a. It consists of a cathode foil, anode foil, electrolytic paper, electrolyte. Here, the oxide layer on the anode foil surface acts as a dielectric. While in contact with the electrolyte, the oxide layer obtains excellent forward insulation property. By etching the foil, surface area is magnified to obtain high capacitance in small volume [1, 5, 6]. An Aluminium Electrolytic Capacitor [AEC] can also be modeled with its electrical properties. Equivalent circuit of an electrolytic capacitor is illustrated in fig. 3b. Where,  $C$  is the Capacitance (F),  $r$  is the Equivalent parallel resistance of anode oxide film ( $\Omega$ ), ESR is the Equivalent Series Resistance ( $\Omega$ ),  $L$  is the Equivalent Series Inductance (H) [6].

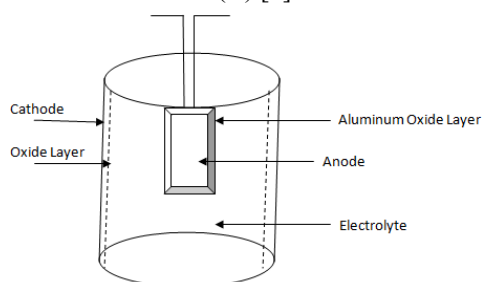


Fig. 3a. Physical Model of Aluminium Electrolytic Capacitor

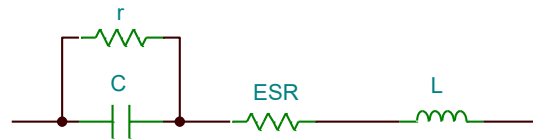


Fig. 3b. Electrical Equivalent Circuit of an Aluminium Electrolytic Capacitor

Output ripple is found to be one of the major health indicators of AEC. In [2] a high-precision, low-cost, and automatic (peak-to-peak value) ripple measurement scheme is proposed utilizing two high-speed comparators and a DAC. By utilizing DAC instead of ADC cost of the system is reduced also portability and automation is illustrated. [3] proposes an online scheme for monitoring buck converters, willing to estimate the  $C$  and ESR of AEC at the output side. The scheme has a relatively low sampling frequency. It uses large-signal load transient trajectories in order to estimate the AEC parameters. Using initial voltage and current step values, the ESR is directly calculated. Then, by utilizing output load voltage trajectory, the capacitor value is calculated [3].

[8] proposes an online estimation method for the calculation of ESR and  $\tan\theta$  (where,  $\theta$  is the loss angle) based on the inductor and capacitor voltage ripples. The derived model is claimed to be applicable for both continuous conduction mode and discrete conduction mode voltage converters. Based on derived models, the online estimation scheme is implemented using wavelet transform denoising (WTD)[8].

In [9] a parameters estimation scheme for AEC is proposed through simulations. This scheme utilizes the sliding mode differentiators and Kalman filter for the online estimation of ESR and capacitance parameters of AEC under noisy conditions. In [10] an on-line parameter measuring scheme for Aluminium Electrolytic Capacitor degradation which involves the Recursive Least Square algorithm with sliding mode differentiators and forgetting factor is proposed. It can concurrently estimate the equivalent capacitance  $C_{eff}$  and the AEC Equivalent Series Resistance (ESR) in noisy current and voltage measurements.

Paper [11] proposes and also experimentally evaluates an online capacitor monitoring algorithm in application to open-end winding topology. Expressions of capacitor current and voltages are derived utilizing a recursive least square method. Paper [14] proposes a monitoring method-based sorting strategy for capacitors in Modular Multilevel Converters (MMC). This paper states the relationship between the capacitor's capacitance, ESR, current and energy. Using the relationship, the capacitances and ESRs of submodule (SM) capacitors are indirectly sorted for the application. In [15], an AEC-monitoring technique utilizing the capacitance and Equivalent Series Resistance (ESR) as the health indicators was built for the power electronic converters used in Photo Voltaic systems.

Schottky diodes are normally assumed to have extra ruggedness and so are less prone to error. However, for better understanding of failure mechanisms of Power Management Unit (PMU), analysis of diodes failure is also important. Fig. 4 represents the electrical and physical model of a Schottky diode

[16]. Failures of diodes are generally categorized as ageing or wear out failures and static, dynamic or catastrophic failures. Diode wear out failures are majorly due to gradual ESD (electrostatic discharges) or any other accumulated wear out. In diodes, catastrophic failures are due to sudden single triggered event like over voltage, excess heat and over current. In [17] a detailed description about diode catastrophic failure and its effect on the PMU is given. However, with an efficient prognostic monitoring unit, the wear out failures can be estimated. Use of SiC Schottky diodes instead of Si Schottky diodes improves the performance of diode by reducing the switching losses, reverse recovery current and temperature dependence [16]. From available literature, AEC degradation is prominent in comparison with the diode degradation in a power converter.

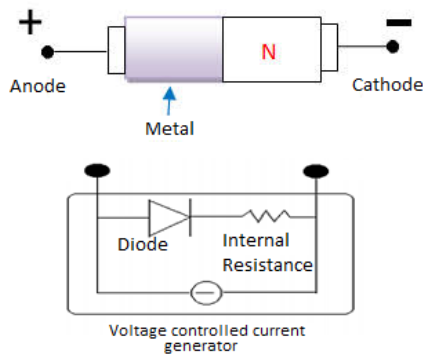


Fig. 4. Physical and electrical representation of Schottky diode

### III. METHODOLOGY

From available literature, it is known that capacitor is the major component leading to failure of SMPS. Thus, degradation analysis of capacitor holds good scope in improving the reliability of power converter. Effective capacitance and ESR are the major parameters of a capacitor which alter with degradation. Output voltage of a power converter is affected by capacitance and ESR values. So, degradation analysis of capacitor can be carried out by monitoring the ripple in output voltage of a DC-DC converter.

With aging and degradation, the effective capacitance of a capacitor reduces. Signature of capacitance reduction is provided by the manufacturer. Likewise, with degradation ESR of the capacitor increases. From literature and according to the industry standards, capacitors are considered completely degraded and not usable in a circuit when it's ESR value reaches 2.8 times of the measured initial ESR value. In case of capacitance, effective capacitance value should not go below 20% of the initial value after which the capacitor is considered to be destructive to be used in the circuit.

The increase in ESR can be modelled by Arrhenius Law as indicated in equation (1)

$$\frac{1}{ESR(t)} = \left(\frac{1}{ESR(0)}\right) \left\{1 - k * t * \exp\left(\frac{-E}{(T+273)}\right)\right\} \quad (1)$$

Where, ESR(t) is the ESR value at time 't', T is the temperature in °C at which the capacitor operates, t is the operating time, ESR(0) is the initial ESR value at t = 0, k is the constant which depends on the design and the construction of

the capacitor, E is the activation energy/ Boltzmann's constant and equals to 4700.

A voltage regulator is designed with external capacitor. By theoretically calculating the variation in capacitance and ESR with aging, degradation analysis is carried out. The degradation of capacitor is measured by monitoring the AC ripple in constant DC output voltage [13]. A detector is designed to aid in the prognostic detection of voltage converter failure due to capacitor failure. Fig. 5 indicates the block diagram of the detector designed. A reference generator is designed to set up the threshold value equivalent to 2.8 times increase in the ESR value above which the voltage ripple is considered to be unacceptable. A peak detector is also designed to identify the AC ripple in the output of voltage regulator. Then an op-amp comparator is designed so as to compare the peak detector output with generated reference voltage.

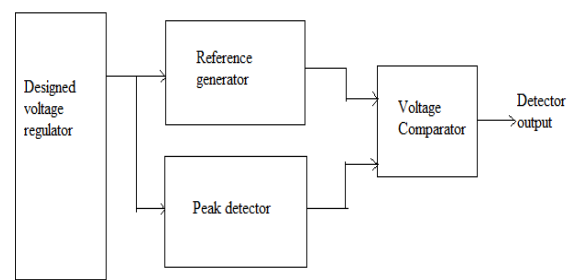


Fig. 5. Detector to monitor the voltage ripple and indicate the voltage regulator failure

### IV. RESULTS AND DISCUSSION

For designing voltage regulator, Texas Instruments LM5085/-Q1 75-V constant on-time PFET buck switching controller is used. LM5085 is a highly efficient automotive grade PFET switching regulator controller. This can be used for the construction of an efficient, low form factored buck converter which can be used in wide range of applications [7]. An effective input voltage of 12 volts which varies between (9-15) V is assumed to design an output voltage regulator which has switching frequency 100 KHz and output voltage of 3.3volts. The voltage regulator designed is depicted in fig. 6.

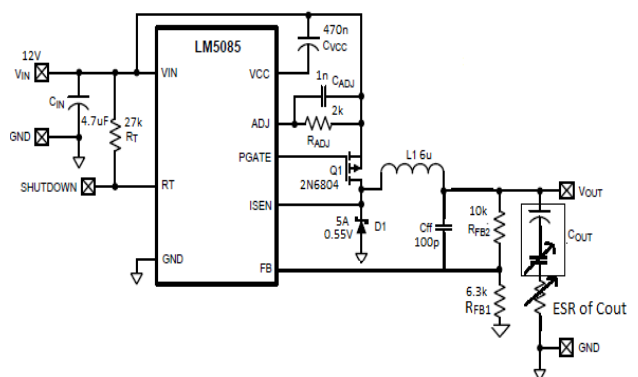


Fig. 6. Voltage regulator to give 3.3V output

A 33uF aluminum Electrolytic capacitor from Nichicon Corporation is used in the design. These capacitors electrical

parameters vary similarly in simulation and experimental setups. To represent degradation, variation of capacitance and ESR of the capacitor are calculated and are represented in Fig. 7a and Fig.7b respectively.

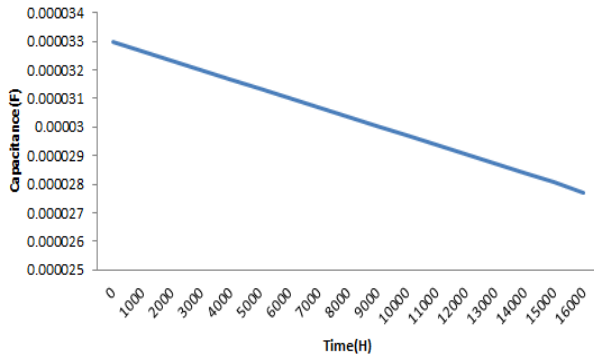


Fig. 7a. Capacitance Change with Time. (Please note that capacitance is in non-logarithmic scale)

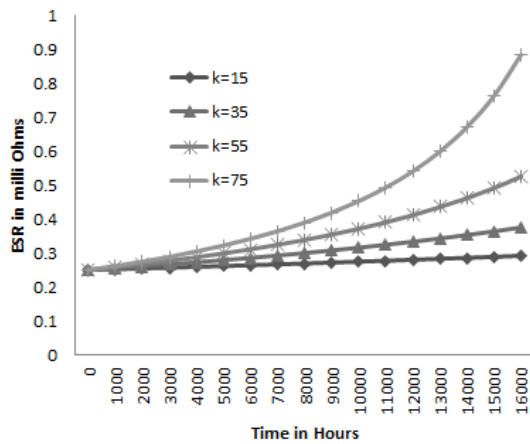


Fig. 7b. Variation of ESR with Time

A thorough theoretical study of how the ESR and capacitance variation affects the performance of voltage regulator is carried out using simulation. Output voltage ripple is a parameter that will vary with varying characteristics of capacitor. For the voltage regulator that is designed, the output ripple is calculated for varied effective capacitance and ESR. Table II lists the variation of effective capacitance, ESR, and output ripple voltage with respect to time. Frequency of Power supply ripple is directly proportional to regulator switching frequency and is characterized by the voltage swing. For facilitating the worst-case condition, simulation is carried out at  $k=75$ . Fig. 8 shows how the output ripple varies with respect to variation in equivalent capacitance and ESR of the capacitor with time. Here, ripple output could be approximated to linear increase as indicated in equation (2)

$$V_{out(p-p)} = I_{(p-p)} * R \quad (2)$$

Where, R is the effective ESR,  $I_{(p-p)}$  is the current through the inductor.

TABLE II  
EFFECTIVE CAPACITANCE, ESR AND OUTPUT RIPPLE VARIATION WITH TIME

Time (Hours)	ESR(t) $\Omega$	Ceff(with time) $\mu$ F	Voutripple (V)
0	2.50E-01	3.30E-05	0.33
1000	2.62E-01	3.27E-05	0.35
2000	2.75E-01	3.23E-05	0.36
3000	2.89E-01	3.20E-05	0.36
4000	3.05E-01	3.17E-05	0.37
5000	3.22E-01	3.14E-05	0.39
6000	3.42E-01	3.10E-05	0.45
7000	3.64E-01	3.07E-05	0.45
8000	3.90E-01	3.04E-05	0.46
9000	4.19E-01	3.00E-05	0.47
10000	4.53E-01	2.97E-05	0.52
11000	4.94E-01	2.94E-05	0.54
12000	5.42E-01	2.90E-05	0.6
13000	6.00E-01	2.87E-05	0.65
14000	6.72E-01	2.84E-05	0.72
15000	7.65E-01	2.81E-05	0.86
16000	8.86E-01	2.77E-05	0.89

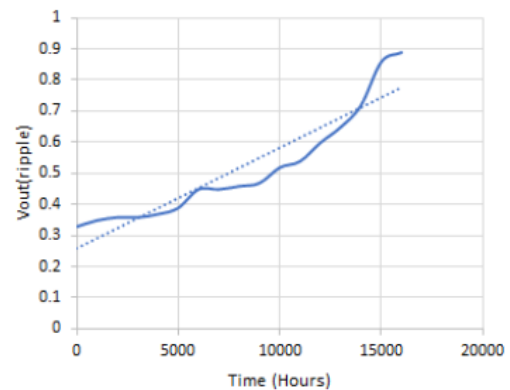


Fig. 8. Variation of Output Voltage Ripple with Time

A detector is designed to aid in the prognostic detection of SMPS failure due to capacitor failure. Then the capacitance and ESR values of the capacitor are modified to emulate the degradation. Regulator output is fed to the detector. Fig. 9a and Fig. 9b indicates the simulation results of voltage regulator with detector for two cases, corresponding to initial capacitor and degraded capacitor parameters. Nomenclature of different parameters considered for simulation are  $V_{reg}$  is the voltage regulator DC output with ripple,  $V_{ref}$  is the reference voltage generated,  $V_{pk}$  is the peak voltage of the regulator output,  $V_{det}$  is the voltage detector output. Table III tabulates the component values considered for simulation and the corresponding results.

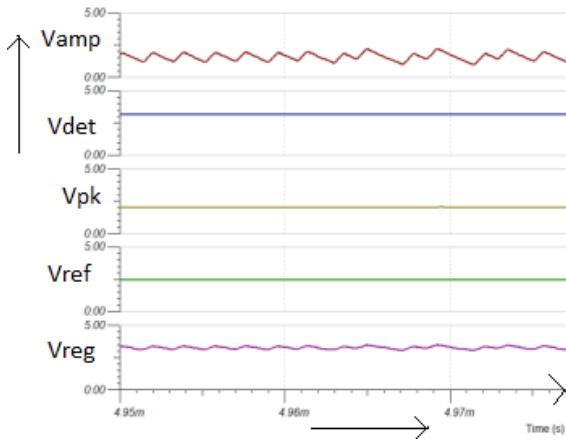


Fig. 9a. Voltage values when capacitor is having its initial values

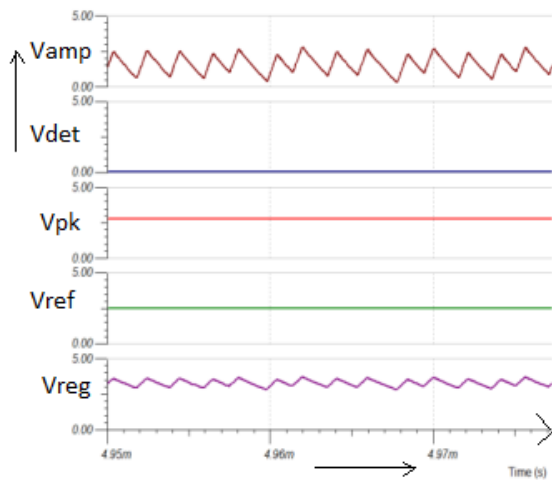


Fig. 9b. Voltage values wherein the ESR was increased to almost 2.8 times the original value

TABLE III

SIMULATION RESULTS OF THE DETECTOR WITH VOLTAGE REGULATOR

Case	Time (hours)	Effective Capacitance (F)	Effective ESR (ohms)	Vreg (only ripple) (V)	Vdet (V)
1	0	33u	250m	0.33	3.15
2	14000	28.4u	670m	0.72	48.27m

From the simulation results we prove that the detector designed works faithfully for the requirement by flipping the output voltage when the set threshold is crossed. Also, the designed detector could be easily implemented and also adaptable for various topologies.

Table IV tabulates the comparison of various methods proposed for the detection of capacitor failure in power supplies. From table IV we can demonstrate that the proposed method is simple, feasible and effective in prognostic detection of power supply failure due to AEC failures.

## V. CONCLUSION AND FUTURE WORK

Switched Mode Power Supplies, or generally termed switchers offer versatile methods of power conversion with high efficiency. But prognostic estimation of the reliability of power converters is very prominent in critical systems. The analysis carried out does the prognostic estimation of capacitor failure by studying the signature of output ripple variation in the power converters. A detector is also designed to indicate the possible near future failure of the converter. These analysis and detector could be utilized to design a fault tolerant DC-DC converter which provides uninterrupted power supply in critical applications.

TABLE IV

COMPARISON OF PROPOSED METHOD WITH EXISTING AEC MONITORING METHODS FOR POWER SUPPLIES

Serial number	Input/Output	Health Indicator	Frequency	Topology	Description of major component/ Function	Tool Used/Approach	Complexity	Reference
1	Not available	Output Ripple	168M	Buck	Low speed DAC, High speed Comparator	Experimental Verification	***	[2]
2	48V/12V	ESR,Ceff	200k	Buck	Load transient trajectory analysis	PSIM simulation, Experimental Verification	**	[3]
3	22V/5V	ESR,Ceff	100k	Buck	Accelerated Aging experiment	Experimental analysis	**	[5]
4	24V/-	ESR,tan $\Theta$	50k	Buck,boost	Wavelet Transform Denoising (WTD)	Matlab simulation	***	[8]
5	200V/100V	ESR,Ceff	10k	Buck	Sliding mode differentiator, Kalman filter [9], Recursive Least Squares [10]	Matlab simulation	***	[9],[10]
6	12/3.3	Output Ripple	100k	Buck	Arrhenius equation to find ESR and Ceff	TINA simulation	*	Proposed work

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