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DESIGN OF NEW ROBUST BACKSTEPPING CONTROL FOR THREE-PHASE GRID-CONNECTED FOUR-LEG SOURCE VOLTAGE PWM CONVERTERS

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Abstract

Due to high performance demands of grid-connected pulse-width modulation (PWM) converters in power applications, backstepping control (BSC) has drawn wide research interest for its advantages, including high robustness against parametric variations and external disturbances. In order to guarantee these advantages while providing high static and dynamic responses, in this work, a robust BSC (RBSC) with consideration of grid-connected PWM converter parameter uncertainties is proposed for three-phase grid-connected four-leg voltage source rectifiers (GC-FLVSR). The proposed RBSC for GC-FLVSR is composed of four independent controllers based on the Lyabonov theory that control DC bus voltage and input currents simultaneously. As a result, unit power factor, stable DC-bus voltage, sinusoidal four-leg rectifier input currents with lower harmonics and zero-sequence (ZS), and natural currents can be accurately achieved. Furthermore, the stability and robustness against load, DC capacitor, and filter inductance variations can be tested. The effectiveness and superiority of the proposed RBSC compared to the PI control (PIC) have been validated by processor-in-the-loop (PIL) co-simulation using the STM32F407 discovery-development-board as an experimental study.

Keywords: three-phase grid-connected four-leg voltage source rectifiers (GC-FLVSR), Robust Backstepping Control (RBSC), parameters uncertainties, harmonic, Zero Sequence Currents (ZSCs), Unit Power Factor (UPF).

1. Introduction

In recent decades, three-phase grid-connected three-leg voltage source rectifiers have been widely used in numerous industrial power applications, such as grid power factor correction, *doubly fed induction generator* (DFIG)-based wind energy systems feeding stand-alone loads, *high-voltage-direct-current* (HVDC) systems, and *electric vehicle* (EV) charging systems [1–3]. They are considered a high-merit system for high-power applications due to their excellent input current quality, *unit power factor* (UPF), controllable DC-bus voltage, and bidirectional power

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flow. However, for several other industrial power applications, the traditional three-leg PWM rectifier may not be an exemplary solution due to the unbalanced single-phase nonlinear loads or the unbalanced grid voltage and asymmetrical impedance [4, 5].

To solve these issues, the utilization of *four-leg PWM voltage source rectifiers* (FLVSR) is highly recommended. These PWM converters are appropriate to maintain balanced sinusoidal grid currents and voltages under all unbalanced conditions and other disturbances [6, 7]. The fourth leg, inserted into the traditional PWM rectifier, provides a *zero-sequence current* (ZSC) path and control and preserves the capability to handle all unbalanced issues [8]. Four-leg PWM converters have commonly been used in stand-alone power generation systems [7], active power filters [9], and distributed static compensators [10].

The control performance and dynamic responses of *grid-connected four-leg voltage source rectifiers* (GC-FLVSR) are strongly dependent on the selected outer DC-bus voltage and inner three-input current controllers. The several controllers that have been developed and used for four-leg converters have the same targets with diverse functionalities [11]. Linear *proportional integral controllers* (PICs) have been proposed to obtain good steady-state performance [12]. However, the ingrained nonlinearities of these four-leg converters and the undesirable disturbances due to parameter changes not only affect the control performance of the PIC [13], but also cause poor dynamic responses in transient-states.

In recent years, several nonlinear techniques have been proposed to improve the control performance and dynamic responses of PWM converters, including *state-space current control* (SSCC) [5], *flatness control* (FC) [13], *sliding mode control* (SMC) [14], *fast terminal sliding mode control* (FTSMC) [15], and *backstepping control* (BSC) [16].

Among the above-mentioned techniques, the classical BSC has been known as an effective and successful technique due to its features of systematic, recursive design, robustness, and better performance under diverse operating conditions. The concept of the classical BSC is to select suitable Lyapunov functions according to the control purposes of all steps of the overall control system [9, 16]. These functions can guarantee the stability and robustness of the control system. Thus, the BSC technique was applied to a three-leg PWM rectifier with the function of controlling both the instantaneous power and DC-bus voltage simultaneously. In [17–19], simulations and experimental results demonstrated that the classical BSC is efficient in terms of stability, robustness, harmonic elimination, disturbance rejection, and power factor correction. A review of the features of BSC in PWM converters is presented in [20]. However, the three-leg converter is still considered the essential converter in the aforementioned works based on the BSC technique. Consequently, the ZSC generated in the case of unbalanced single-phase loads and grid voltages is not considered, and the PWM converter parameter uncertainties are not taken into account in the theoretical framework of the classical BSC technique, so control system robustness cannot be guaranteed.

In this paper, a *robust backstepping control* (RBSC) technique with consideration of GC-FLVSR uncertainties is proposed to control the DC-bus voltage and input currents of GC-FLVSR in the dq0 frame under diverse operating conditions such as DC-bus voltage change, load change, and parameter variations. The four-leg PWM rectifier is adopted here for its capacity to provide a ZSC path and regulation and thus avoid grid voltage fluctuation. In this paper, the transient and steady state control performances of the proposed RBSC are evaluated and compared with those based on the traditional PIC in terms of reference tracking, integral performance, DC-bus voltage stabilization, input current harmonic and ZSC eliminations, power factor correction, and neutral current mitigation. The proposed RBSC technique provides favourable and satisfactory results for all previous control performance indicators that confirm the superiority and effectiveness of the proposed control strategy.

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The rest of this paper is organized as follows: in Section 2, the dynamic model of the 3P-4LR is presented. Then, detailed DC-bus voltage and input current control loops based on the proposed RBSC technique are developed and detailed in Section 3. Section 4 presents the PIL co-simulation results and discusses the viability and effectiveness of the proposed RBSC technique for 3P–4LR. Finally, Section 5 summarizes the contributions of this work.

2. Modelling of three-phase GC-FLVSR

The three-phase FLVSR connected to the grid through filter inductors (L_{fabcn}) with parasitic resistances (R_{fabcn}) is shown in Fig. 1. The grid is presented by three sinusoidal voltages (e_{abc}) and a grid neutral line in series with four inductors (L_{gabcn}) that have internal resistances (R_{gabcn}) and are connected with the load through the DC capacitor (C_{dc}). The grid currents, input currents, and input voltages are i_{gabcn}, i_{fabcn}, and v_{fabcn} respectively. I_L, I_c, I_{dc}, and V_{dc} are the load current, capacitor current, DC current, and DC voltage, respectively.

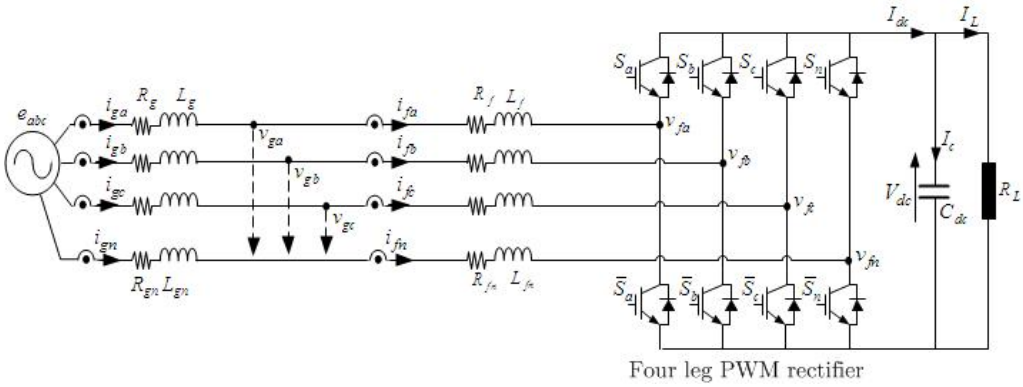

Fig. 1. Structure of the three-phase grid-connected four-leg voltage source rectifier (GC-FLVSR).

To facilitate the controller design, the model of FLVSR is given in dq0 frame [13] as:

$$\begin{cases} \dfrac{\mathrm{d}i_{fd}}{\mathrm{d}t} = -\dfrac{R_f}{L_f} i_{fd} + \omega i_{fq} - \dfrac{v_{gd}}{L_f} + \dfrac{v_{fd}}{L_f} \\ \dfrac{\mathrm{d}i_{fq}}{\mathrm{d}t} = -\dfrac{R_f}{L_f} i_{fq} - \omega i_{fd} - \dfrac{v_{gq}}{L_f} + \dfrac{v_{fq}}{L_f} \\ \dfrac{\mathrm{d}i_{f0}}{\mathrm{d}t} = -\dfrac{(R_f + 3L_n)}{(L_f + 3L_n)} i_{f0} - \dfrac{v_{g0}}{(L_f + 3L_n)} + \dfrac{v_{f0}}{(L_f + 3L_n)} \\ \dfrac{\mathrm{d}V_{dc}^2}{\mathrm{d}t} = \dfrac{2V_{gd}}{C} i_{fd} - \dfrac{2V_{dc}^2}{CR_L} \end{cases}, \tag{1}$$

where: i_{fdq0} and v_{fdq0} are the active, reactive, and ZS input currents and voltages, respectively. ω is the grid angular frequency. According to (1), there are coupling terms between i_{fd} and i_{fq}.

These terms are mitigated by introducing the decoupling variables u_d and u_q as follows:

$$\begin{cases} \underbrace{u_d}_{\text{feedback}} = -\left(L_f \dfrac{\mathrm{d}i_{fd}}{\mathrm{d}t} + R_f i_{fd}\right) \\ \underbrace{u_q}_{\text{feedback}} = -\left(L_f \dfrac{\mathrm{d}i_{fq}}{\mathrm{d}t} + R_f i_{fq}\right) \\ u_0 = -\left((L_f + 3L_n)\dfrac{\mathrm{d}i_{f0}}{\mathrm{d}t} + (R_f + 3R_n) i_{f0}\right) \\ u_{dc} = i_{fd} = \dfrac{C}{2V_{gd}}\left(\dfrac{\mathrm{d}V_{dc}^2}{\mathrm{d}t} + \dfrac{2V_{dc}^2}{CR_L}\right) \end{cases}. \tag{2}$$

The FLVSR input voltages or the control input variables v^*_{fdq0} in the dq0 frame are given as:

$$\begin{cases} \underbrace{v^*_{fd}}_{\text{feedback}} = u_d + \underbrace{\omega L_f i_{fq} + V_{g\max}}_{\text{feedforward}} \\ \underbrace{v^*_{fq}}_{\text{feedback}} = u_q - \underbrace{\omega L_f i_{fd}}_{\text{feedforward}} \\ v^*_{f0} = u_0 \\ i^*_{fd} = u_{dc} \end{cases}. \tag{3}$$

From (1), it is clear that the ideal GC-FLVSR when the uncertainties are not considered consists of four dynamic models, DC voltage and three input currents. In the next section, we are rearranging these dynamic models for the case when the uncertainties were considered as bellow.

2.1. Dynamic model of DC bus voltage and active input current

From (1), the square DC voltage dynamic, considering its uncertainty, can be expressed as:

$$\begin{aligned} \frac{\mathrm{d}V_{dc}^2}{\mathrm{d}t} &= a_{dc}V_{dc}^2 + b_{dc}u_{dc} \\ &= (a_{dc} + \Delta a_{dc})V_{dc}^2 + (b_{dc} + \Delta b_{dc})u_{dc}, \\ &= a_{dc}V_{dc}^2 + b_{dc}u_{dc} + \psi_{dc}(t) \\ \psi(t) &= \Delta a_{dcn}V_{dc}^2 + \Delta b_{dcn}u_{dc} \end{aligned} \tag{4}$$

where: $a_{dc} = -\dfrac{2}{C_{dc}Z_L}$, $b_{dc} = \dfrac{2v_{g\max}}{C_{dc}}$. a_{dcn} and b_{dcn} are the nominal values of a_{dc} and b_{dc}, respectively. Δa_{dcn} and Δb_{dcn} are the parameter variations. $\psi_{dc}(t)$ is the DC bus voltage dynamic model uncertainty function, whose limit value is given as $|\psi_{dc}(t)| < \delta_{dc}$.

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When the active input current dynamic uncertainty is considered, (1-a) can be rewritten as:

$$\begin{aligned}\frac{\mathrm{d}i_{fd}(t)}{\mathrm{d}t} &= a_d i_{fd}(t) + b_d u_d(t)\\ &= (a_{dn} + \Delta a_{dn}) i_{fd}(t) + (b_{dn} + \Delta b_{dn}) u_d(t)\\ &= a_{dn} i_{fd}(t) + b_{dn} u_d(t) + \psi_d(t)\\ \psi_d(t) &= \Delta a_{dn} i_{fd}(t) + \Delta b_{dn} u_d(t)\end{aligned}, \tag{5}$$

where: $a_d = -\dfrac{R_f}{L_f}$, $b_d = -\dfrac{1}{L_f}$. a_{dn} and b_{dn} are the nominal values of a_d and b_d respectively. $\psi_d(t)$ is the active input current dynamic uncertainty function whose limit value is supposed to be given as $|\psi_d(t)| < \delta_d$.

2.2. Dynamic model of reactive input current

When the reactive input current dynamic uncertainty is considered, (1-b) can be rewritten as:

$$\begin{aligned}\frac{\mathrm{d}i_{fq}(t)}{\mathrm{d}t} &= a_q i_{fq}(t) + b_q u_q(t)\\ &= (a_{qn} + \Delta a_{qn}) i_{fq}(t) + (b_{qn} + \Delta b_{qn}) u_q(t)\\ &= a_{qn} i_{fq}(t) + b_{qn} u_q(t) + \psi_q(t)\\ \psi_q(t) &= \Delta a_{qn} i_{fq}(t) + \Delta b_{qn} u_q(t)\end{aligned}, \tag{6}$$

where: $a_q = -\dfrac{R_f}{L_f}$, $b_q = -\dfrac{1}{L_f}$. a_{qn} and b_{qn} are the nominal values of a_q and b_q respectively. $\psi_q(t)$ is the reactive input current dynamic uncertainty function whose limit value is supposed to be given as $\left|\psi_q(t)\right| < \delta_q$.

2.3. Dynamic model of zero sequence input current

When the ZSC dynamic uncertainty is considered, (1-c) becomes:

$$\begin{aligned}\frac{\mathrm{d}i_{f0}(t)}{\mathrm{d}t} &= a_0 i_{f0}(t) + b_0 u_0(t)\\ &= (a_{0n} + \Delta a_{0n}) i_{f0}(t) + (b_{0n} + \Delta b_{0n}) u_0(t)\\ &= a_{0n} i_{f0}(t) + b_{0n} u_0(t) + \psi_0(t)\\ \psi_0(t) &= \Delta a_{0n} i_{f0}(t) + \Delta b_{0n} u_0(t)\end{aligned}, \tag{7}$$

where: $a_0 = -\dfrac{(R_f - 3R_n)}{(L_f - 3L_n)}$, $b_0 = -\dfrac{1}{(L_f - 3L_n)}$, a_{0n}, and b_{0n} are the nominal values of a_0 and b_0 respectively. $\psi_0(t)$ is the ZSC dynamic uncertainty function whose limit is given as $|\psi_0(t)| < \delta_0$ and δ_{dc}, δ_d, δ_q, and δ_0 are positive constants.

3. Proposed RBSC technique for GC-FLVSR

3.1. RBSC for DC-bus voltage and active input current

By controlling the DC-bus voltage and active input current, two main objectives are addressed. One is to force the square of V_{dc} ($V_{dc}^2 = x_v$) to track its reference ($V_{dc}^{*2} = x_v^*$) and to provide

the active input current reference (i^*_{fd}) used in the active input current control loop. The other objective is to force the active input current i_{fd} to track its reference with zero steady state error to obtain the active input voltage reference v^*_{fd}.

The DC-bus voltage error is defined as $e_v = x_v - x^*_v$, and its derivative $\dot{e}_v$ can be expressed as:

$$\dot{e}_v = \dot{x}_v - \dot{x}^*_v. \tag{8}$$

In order to enforce the DC-bus voltage error e_v to converge to zero asymptotically, a Lyapunov function defined as $V_v = \frac{1}{2}e_v^2$ is selected and its derivative is expressed as:

$$\dot{V}_v = e_v(\dot{x}_v - \dot{x}^*_v). \tag{9}$$

Substituting $\dot{x}_v$ from (4) into (9) results in:

$$\dot{V}_v = e_v\left(a_{dc}x_v + b_{dc}u_{dc} + \psi_{dc}(t) - \dot{x}^*_v\right). \tag{10}$$

The stability of V_{dc} control loop is ensured when the derivative of $\dot{V}_v$ given in (9) is strictly negative definite. For this, the term $(a_{dc}x_v + b_{dc}u_{dc} + \psi_{dc}(t) - \dot{x}^*_v)$ can be expressed as [19]:

$$\left(a_{dc}x_v + b_{dc}u_{dc} + \psi_{dc}(t) - \dot{x}^*_v\right) = -k_{dc}e_v - \delta_v \mathrm{sgn}(e_v) + \psi_{dc}(t). \tag{11}$$

The derivative of Lyapunov function $\dot{V}_v$ given in (10) becomes:

$$\dot{V}_v = -k_{dc}e_v^2 - e_v\left(\delta_v \mathrm{sgn}(e_v) - \psi_{dc}(t)\right). \tag{12}$$

From (12), $\dot{V}_v$ is strictly negative when $\delta_v > |\psi_{dc}(t)|$ is satisfied.

As can be observed, $\dot{V}_v$ will be strictly negative as long as $\delta_v > |\psi_{dc}|$, which confirms that the e_v will converge to zero and the stability of V_{dc} control loop can be guaranteed.

From (12), the control variable $u_{dc} = i^*_{fd}$ of the V_{dc} control loop can written as follows:

$$i^*_{fd} = u_{dc} = \frac{1}{b_{dc}}\left(-k_v e_v - a_{dc}x_v - \delta_v \mathrm{sgn}(e_v) + \dot{x}^*_v\right). \tag{13}$$

In the active input current control loop, the term $x_d = i_{fd}$ can be used as a state variable and $u_d(t)$ as a decoupling variable. For this, the derivative of $e_d = x_d - x^*_d$ is expressed as:

$$\dot{e}_d = \dot{x}_d - \dot{x}^*_d = \dot{x}_d - \dot{x}^*_d. \tag{14}$$

In order to enforce the tracking error e_d to zero asymptotically, the corresponding Lyapunov function is defined as $V_d = \frac{1}{2}e_d^2$, and its derivative can be expressed as:

$$\dot{V}_d = e_d\left(\dot{x}_d - \dot{x}^*_d\right). \tag{15}$$

Substituting $\dot{x}_d$ from (5) into (15) results in:

$$\dot{V}_d = e_d(a_{dn}i_{fd}(t) + b_{dn}u_d(t) + \psi_d(t) - \dot{x}^*_d). \tag{16}$$

To guarantee the stability of the active input current control loop under the parameter uncertainties, the term $(a_{dn}i_{fd}(t) + b_{dn}u_d(t) + \psi_d(t) - \dot{x}^*_d)$ in (16) must be expressed as:

$$a_{dn}i_{fd}(t) + b_{dn}u_d(t) + \psi_d(t) - \dot{x}^*_d = -k_d e_d - \delta_d \mathrm{sgn}(e_d) + \psi_d(t). \tag{17}$$

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By substituting (17) into (16), (16) becomes:

$$\dot{V}_d = -k_d e_d^2 - e_d(\delta_d \text{sgn}\,(e_d) - \psi_d(t)). \tag{18}$$

According to (18), $\dot{V}_d$ is strictly negative when $\delta_d > |\psi_d(t)|$ is satisfied.
According to (17), the decoupling control variable u_d is expressed as:

$$u_d(t) = \frac{1}{b_{dn}}(-a_{dn}x_d - k_d e_d - \delta_d \text{sgn}\,(e_d) + \dot{x}_d^*). \tag{19}$$

By using (1-a), the active input reference voltage $v_{f\,d}^*$ can be expressed as:

$$v_{f\,d}^* = \frac{1}{b_{dn}}(-a_{dn}x_d - k_d e_d - \delta_d \text{sgn}\,(e_d) + \dot{x}_d^*) + L_f \omega x_q + v_{gd}. \tag{20}$$

3.2. BSC for reactive input current

The objective of this subsystem is to force the reactive input current error ($e_q = x_q - x_q^*$) to zero to provide a high power factor under reactive input current dynamic model uncertainties. The derivative $\dot{e}_q$ of this tracking error is expressed as:

$$\dot{e}_q = \dot{x}_q - \dot{x}_q^*. \tag{21}$$

In order to enforce e_q to zero, V_q is defined as $V_q = \frac{1}{2}e_q^2$, and its derivative is thus written as:

$$\dot{V}_q = e_q(\dot{x}_q - \dot{x}_q^*). \tag{22}$$

Substituting $\dot{x}_q$ from (6) into (22), it results in:

$$\dot{V}_q = e_q(a_{qn}x_q + b_{nq}u_q - \dot{x}_q^* + \psi_q(t)). \tag{23}$$

To guarantee that $\dot{V}_q < 0$, the term $(a_{qn}x_q + b_{nq}u_q - \dot{x}_q^* + \psi_q(t))$ must be expressed as:

$$a_{qn}x_q + b_{qn}u_q(t) - \dot{x}_q^* + \psi_q(t) = -k_q e_q - \delta_q \text{sgn}\,(e_q) + \psi_q(t). \tag{24}$$

By substituting (24) into (23), (23) becomes:

$$\dot{V}_q = -k_q e_q^2 - \delta_q e_q \text{sgn}\,(e_q) + e_q \psi_q(t). \tag{25}$$

This derivative is strictly negative when $\delta_q > |\psi_q|$ is satisfied.
From (25), the decoupling control variable u_q is given as follows:

$$u_q = \frac{1}{b_{qn}}(-a_{qn}x_q - k_q e_q - \delta_q \text{sgn}\,(e_q)), \tag{26}$$

$$v_{f\,q}^* = \frac{1}{b_{qn}}(-a_{qn}x_q - k_q e_q - \delta_q \text{sgn}\,(e_q)) - \omega L_f i_{f\,d} + v_{gq}. \tag{27}$$

3.3. BSC for zero sequence input current

The objective of this subsystem is to force the ZSC ($x_0 = i_{f0}$) to tend to zero with zero transient and steady state errors to mitigate the neutral current oscillation. The error of this current is defined as $e_0 = x_0 - x_0^*$, and its derivative is expressed as:

$$\dot{e}_0 = \dot{x}_0 - \dot{x}_0^*. \tag{28}$$

The Lyapunov function V_0 is defined as $V_0 = \frac{1}{2}e_0^2$, and its derivative can be expressed as:

$$\dot{V}_0 = e_0\dot{e}_0, \tag{29}$$

$$\dot{V}_0 = e_0(a_{0n}x_0 + b_{n0}u_0 + \psi_0(t)). \tag{30}$$

To guarantee the stability of this loop, $(a_{0n}x_0 + b_{n0}u_0 + \psi_0(t))$ must be expressed as:

$$a_{0n}x_0 + b_{n0}u_0 + \psi_0 = -k_0e_0 - \delta_0\text{sgn}(e_0) + \psi_0(t), \tag{31}$$

where, k_V, k_d, k_q, and k_0 are positive constants.

By substituting (31) into (30), (30) becomes:

$$\dot{V}_0 = -k_0e_0^2 - \delta_0e_0\text{sgn}(e_0) + e_0\psi_0(t). \tag{32}$$

This derivative is strictly negative when $\delta_0 > |\psi_0|$ is satisfied.

From (31), the decoupling control variable of this control loop u_0 is given as follows:

$$u_0 = \frac{1}{b_{n0}}(-a_{0n}x_0 - k_0e_0 - \delta_0\text{sgn}(e_0)), \tag{33}$$

$$v_{f0}^* = \frac{1}{b_{n0}}(-a_{0n}x_0 - k_0e_0 - \delta_0\text{sgn}(e_0)) + v_{g0}\,. \tag{34}$$

The advantages of the proposed RBSC over other traditional BSC are explained as follows:

The roles of the terms $-k_ve_v$ in (13), $-k_de_d$ in (20), $-k_qe_q$ in (27) and $-k_0e_0$ in (34) are useful to minimize the chattering phenomena in the proposed RBSC efforts because the terms $-k_ve_v^2$ in (12), $-k_de_d^2$ in (19), $-k_qe_q^2$ in (26) and $-k_0e_0^2$ in (33) will guarantee the negative value of the $\dot{V}_v < 0$and $\dot{V}_{dq0} < 0$ even in the worst cases when $\delta_v < |\psi_v(t)|$, $\delta_d < |\psi_d(t)|$, $\delta_q < |\psi_q(t)|$ and $\delta_0 < |\psi_0(t)|$. On the other hand, δ_{vdq0} can be accurately and conservatively chosen to avert the increase in the chattering phenomenon resulting from the terms $\delta_v\text{sgn}(e_v)$ in (12), $\delta_d\text{sgn}(e_d)$ in (19), $\delta_q\text{sgn}(e_q)$ in (26) and $\delta_0\text{sgn}(e_0)$ in (33).

The proposed RBSC for GC-FLVSR is illustrated in Fig. 2. As it is shown, the input voltage references are provided by the inner loop controllers, and the outer loop controller is used to preserve a constant DC-bus voltage and provide a suitable active input current reference ($x_d^* = i_{fd}^*$). The 3D-SVPWM method described in [9, 10] is applied in this work because of its significant advantages of constant switching frequency, low input voltage and current harmonics, high DC-bus voltage utilization, and low DC-bus voltage ripple.

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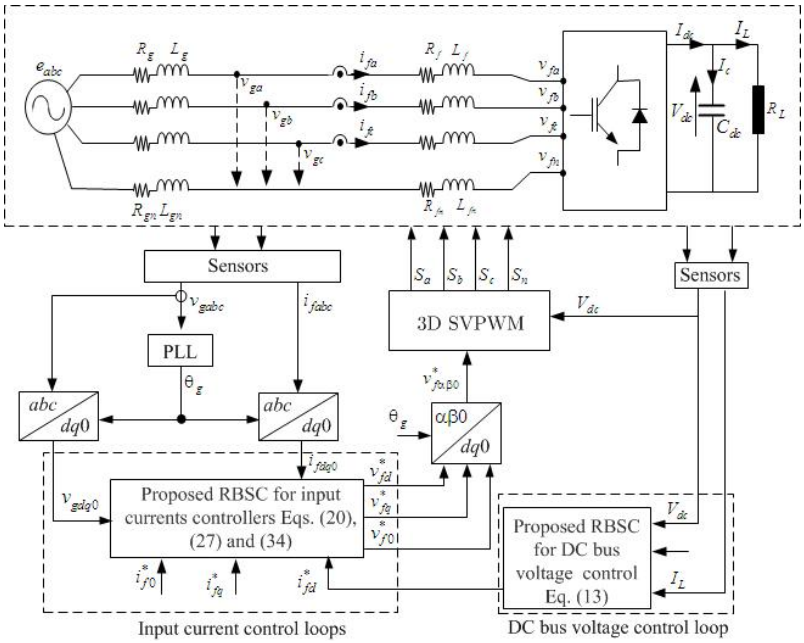

Fig. 2. Proposed RBSC schematic of a three phase grid-connected four-leg voltage source rectifier.

4. Processor-in-the-Loop (PIL) co-simulation and performance evaluation of the proposed control strategy

In order to validate the viability, performance, and effectiveness of the proposed RBSC for GC-FLVSR under parameter uncertainties, a PIL co-simulation of the system has been performed using an STM32F407 discovery-development-board in an experimental study based on the Euler method with a sample period of 10^{-6}s using PowerGUI in the Simulink model. The co-simulation scenario studies were conducted for the proposed RBSC strategy to study two aspects: a) the effects of the proposed RBSC on response time, reactive power compensation, harmonics and ZSC mitigations, and DC voltage regulation; and b) the robustness and stability of the proposed RBSC under the variations of DC bus voltage, load, DC capacity, and filter inductors. The system and simulation parameters are given in Table 1.

Some PIL co-simulation results of the proposed RBSC and the PIC are provided for comparison. In addition, the errors of the DC-bus voltage and input currents are also represented and analysed in terms of performance integral criteria such as *Integral-Time-Absolute-Error* (ITAE) and *Integral-Time-Square-Error* (ITSE) [21]. These error performance indexes of the control outputs x (V_{dc}, i_{fd}, i_{fq} and i_{f0}) and their references x^* are defined as:

$$\begin{cases} \text{ITAE} = \displaystyle\int_0^t t\,|x - x^*|\,\mathrm{d}t \\ \text{ITSE} = \displaystyle\int_0^t t(x - x^*)^2\,\mathrm{d}t \end{cases}. \tag{35}$$

Table 1. Values of system and co-simulation parameters.

Parameter	Value
AC grid voltage	220 V
Fundamental frequency of grid voltage	50 Hz
DC-bus voltage V_{dc}	700 V
Capacitor of DC side rectifier C_{dc}	3 mF
DC load resistance R_L	100 Ω
Input filter inductances L_f, L_{fn}	2 mH, 1 mH
Input filter resistances R_f, R_{fn}	0.15 Ω
Grid inductances L_g, L_{gn}	0.1 mH, 0.05 mH
Grid resistances R_g, R_{gn}	0.1 Ω
Sampling period of simulation	10^{-6} s
Switching frequency f_s	16 kHz

The microcontroller of this discovery-development-board is the STM32F407VG, which features 1 Mb of flash memory, ARM®-Cortex®-M4F-CPU 32-bit architecture, *Floating Point Unit* (FPU), *Digital-Signal-Processor* (DSP), and 192KB SRAM with a maximum operational frequency of 168 MHz [22]. In Fig. 3, the proposed control technique for GC-FLVSR employing the STM32F407 discovery-development board is shown with its PIL structure.

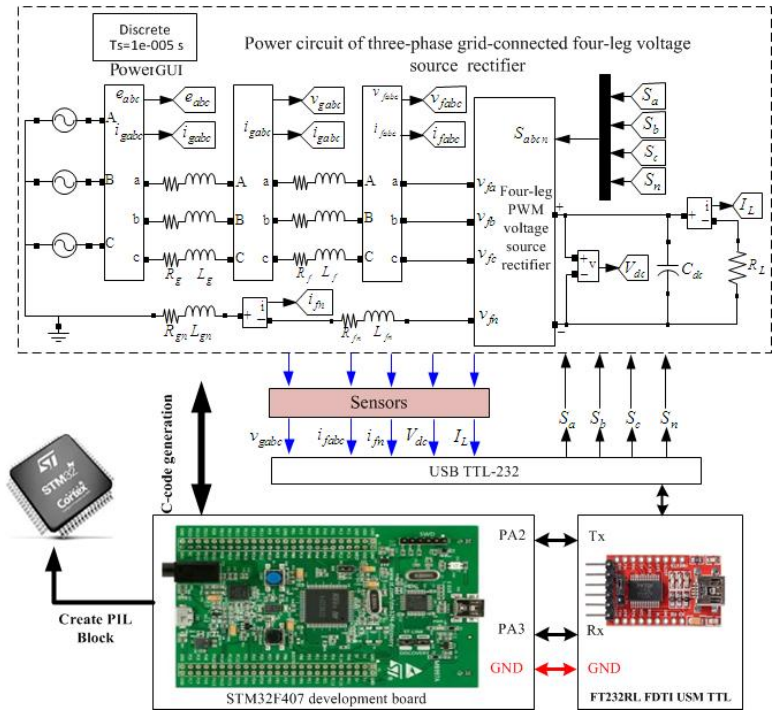

Fig. 3. PIL co-simulation of the proposed RBSC-based grid-connected four-leg voltage source rectifier.

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The implementation of the proposed control strategy for GC-FLVSR is carried out by consolidating all sub-control algorithms into a new single control circuit and defining the used microcontroller discovery-development-board in the system simulation as well as the inputs/outputs of the control circuit in MATLAB/Simulink. The algorithms in the control circuit are converted into C code using the embedded coder installed from MathWorks on the host PC that contains the Simulink model which, in turn, is uploaded into the STM32F407 development-board for flashing the compiled proposed control strategy to the microcontroller using a serial connection interface (YP-05 FTDI F232RL adapter) as shown in Fig 3. We integrate the previously generated C code in the PIL block into a new Simulink model to run the proposed control strategy on the STM32F407 development board [22]. After that, to control the system, the microcontroller computes the GC-FLVSR's state vectors and sends them to the host PC, which controls the Simulink power circuit of the GC-FLVSR via the same serial connection interface for operating it (Fig. 3).

4.1. Test 1 – Ideal operating conditions

The comparative study of control performances of both controllers (PIC and proposed RBSC) was first carried out under ideal conditions and nominal values of the DC capacitor and filter inductors, as depicted in Figs. 4 (a to d). The integral error performance indexes (ITAE and ITSE) values for each controller were analysed and illustrated in Table 2. Also, the FLVSR dynamic responses for both strategies are represented in Figs. 4(a and b).

Table 2. Comparative study of both control strategies of GC-FLVSR responses when the DC capacitor is 3 µF.

	Errors	**PIC**	**Proposed RBSC**
ITAE	e_v	$3.925 \cdot 10^{-4}$	$8.415 \cdot 10^{-5}$
	e_d	$8.914 \cdot 10^{-3}$	$1.520 \cdot 10^{-3}$
	e_q	$5.265 \cdot 10^{-3}$	$1.141 \cdot 10^{-3}$
	e_0	$3.734 \cdot 10^{-3}$	$1.003 \cdot 10^{-3}$
ITSE	e_v	$3.275 \cdot 10^{-5}$	$4.354 \cdot 10^{-7}$
	e_d	$6.864 \cdot 10^{-3}$	$1.281 \cdot 10^{-3}$
	e_q	$4.931 \cdot 10^{-3}$	$1.902 \cdot 10^{-4}$
	e_0	$3.503 \cdot 10^{-3}$	$3.301 \cdot 10^{-4}$

According to these figures, it is clear that the DC-bus voltage and input currents reach their reference values with faster responses (0.01 s) and overshoots at the start of the FLVSR and with very small values of oscillations using the proposed RBSC strategy as shown in Figs. 4 and Table 2. In addition, the error indexes are much smaller than those of the PIC strategy, which demonstrates that the proposed RBSC strategy yields better performance and has the ability to enhance the integral error performance indexes compared to those based on the PIC. It should be noted that the proposed RBSC strategy is defined as the strategy that reduces those indexes.

The grid currents (i_{gabcn}), the first-phase grid voltage and its corresponding current, and the harmonic spectrum of grid currents using both control strategies are illustrated in Figs. 5. It can be observed from these figures that the grid currents are sinusoidal with lower oscillations using the proposed RBSC strategy and the maximum neutral grid current oscillation is also perfectly reduced from 1 A using the PIC strategy to 0.3 A using the proposed RBSC strategy. The grid currents are in phase with their corresponding grid voltages, which demonstrates that the maintained grid UPF is accurately achieved and the absorption of the sinusoidal currents is

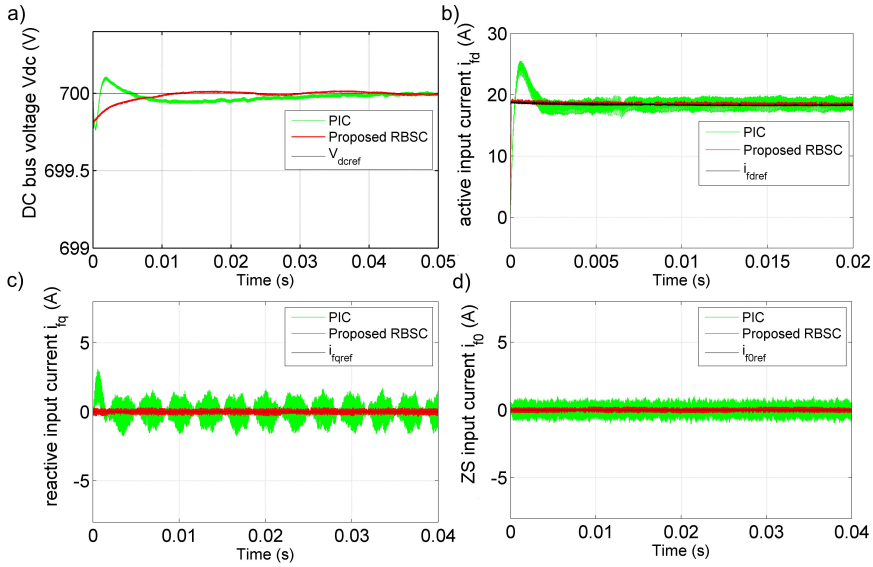

Fig. 4. Comparison of DC bus voltage and input currents performance when the DC capacitor is 3 μF.

also guaranteed under this transient. The total harmonic distortion (THD) is 2.24% when using the PIC strategy, but it is reduced to 0.77% when using the proposed RBSC strategy, as shown in Fig. 5c, which meets the IEEE 519 standard for current distortion limits.

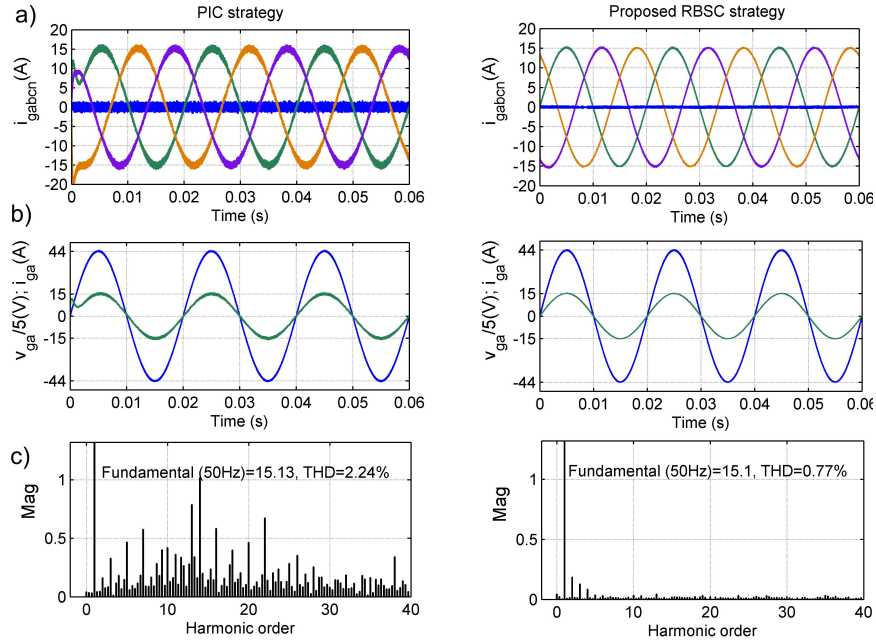

Fig. 5. Grid currents, first-phase grid voltage and its corresponding current, and the harmonic spectrum of grid currents under ideal parameters. PIC strategy (on left), proposed RBSC strategy (on right).

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4.2. Test 2 – Change of DC-bus voltage

The second comparative study is performed through a test of DC bus voltage step change from 700 V to 750 V at 0.05 s, and the control performance of both control strategies is represented in Figs. 6 (a, b, c, and d). These figures compare the performance of the DC bus voltage and input currents before and after this change when the DC capacitor is 3 µF.

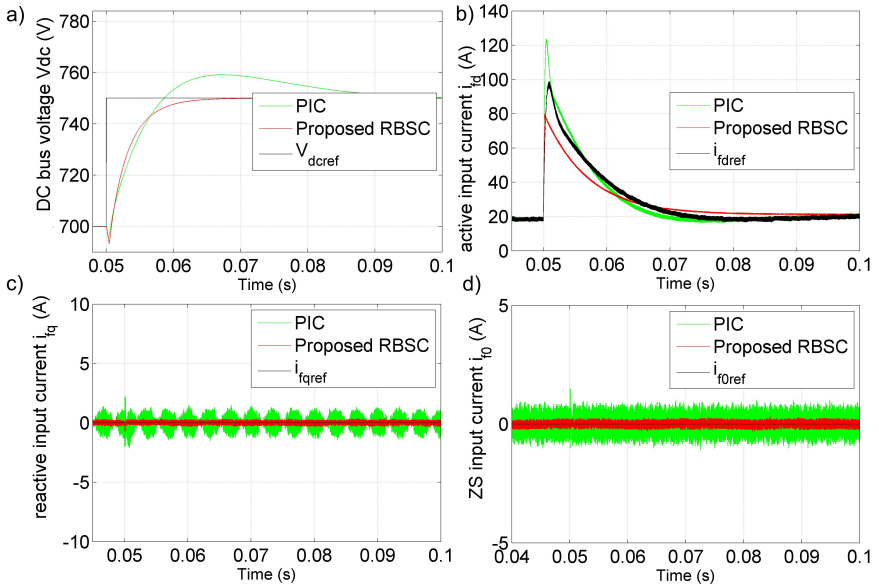

Fig. 6. Comparison of DC bus voltage and input currents performance under DC-bus voltage reference change from 700 V to 750 V at 0.05s when the DC capacitor is 3 µF.

When using the proposed RBSC, the DC-bus voltage has a very fast response (0.01 s) and tracks its reference value without an overshoot after the change and with very small oscillations after this change. The traditional PIC has an overshoot of 12 V and a settling time of 0.05 s, while the proposed RBSC has a zero overshoot and a response time of 0.01 s. The active input current reaches its reference value exactly and fast, with a fast transient time at this change and with very small oscillations after this change. The maximum overshoot of this current at the change is 125 A when using the PIC, which is significantly reduced to 80 A using the proposed RBSC.

The reactive and ZS current are kept constants at zero before and after this change and are not affected by this change, and their oscillations are very small when using the proposed RBSC strategy, which demonstrates that the grid UPF operation and the perfect decoupling of input currents as well as active and reactive powers have been accurately achieved using the proposed RBSC strategy.

4.3. Test 3 – Load change

In this test scenario, a load resistance variation is achieved from 100 to 50 Ω at 0.05 s to evaluate both control strategies performance under a 100% decrease in load resistance power. The control parameters are the same as in Test 1. Figs. 7 and 8 show the control performance and dynamic responses for both control strategies for GC-FLVSR.

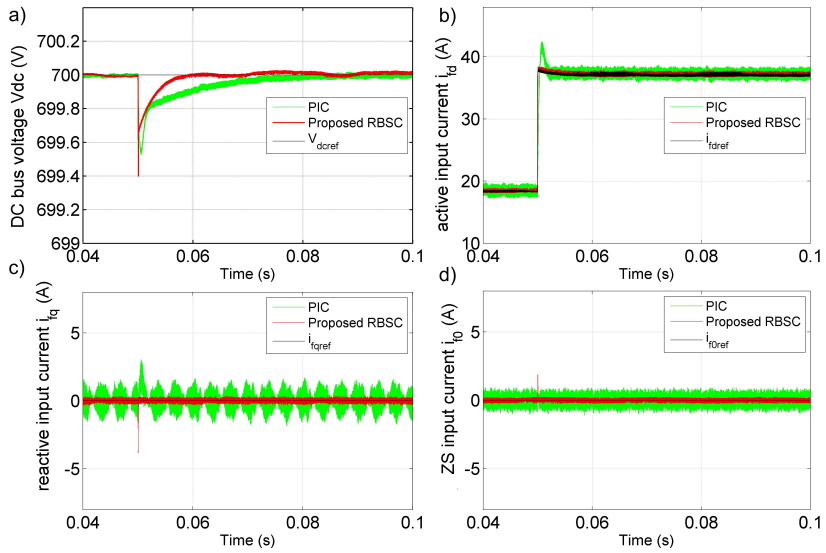

Fig. 7. Comparison of FLVSR performance with the traditional PIC strategy and the proposed RBSC strategy under load change from 100 to 50 Ω at 0.05s with ideal parameters.

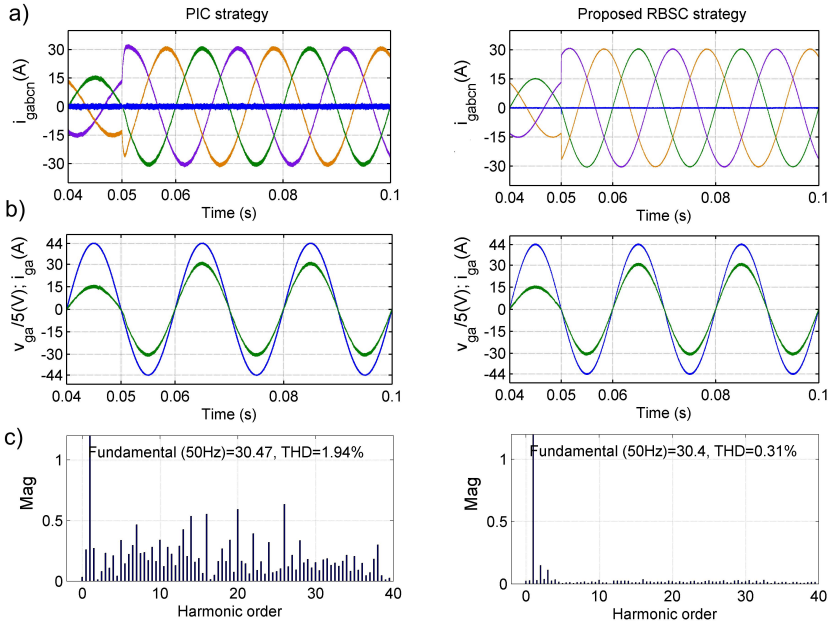

Fig. 8. Grid currents, first-phase grid voltage and its corresponding current, and the harmonic spectrum of grid currents under load change from 100 to 50 Ω at 0.05 s. PIC strategy (on left), proposed RBSC strategy (on right).

As shown in Fig. 7a, the load change causes an undershoot in the DC-bus voltage under both strategies. When the proposed RBSC is used, the DC-bus voltage remains constant near its reference value, and the undershoot is compensated after a very short transient period by

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increasing the active input current as well as the active power, so that the active input current reaches its new reference value with high accuracy, stability, and very small oscillations, as shown in Fig. 7b, which demonstrates the high disturbance rejection ability of the proposed RBSC. When the proposed RBSC is compared to the PIC, the reactive and zero-sequence input currents oscillate around zero with very small oscillations, as shown in Figs. 7c and (d), confirming that the proposed RBSC ensures accurate decoupling of active and reactive input currents as well as powers.

The grid currents (i_{gabc}), the first phase grid voltage and its corresponding current, and the grid current THD values under both control strategies are illustrated in Figs. 8a, b, and c, respectively. It can be observed from these figures that the grid currents have sinusoidal waveforms and can be kept in phase with their corresponding voltages, guaranteeing a UPF operation of the FLVSR. The THD values of the grid currents under load power change are significantly reduced from 1.94% under the traditional PIC to 0.31% using the proposed RBSC strategy, which fits the IEEE 519 standard for current distortion limits.

4.4. Test 4 – Robustness against parameters variations

In the first scenario of this test, the DC capacity C_{dc} was increased to 6 µF to evaluate the robustness and the disturbance rejection ability of the proposed RBSC under a 100% decrease in load resistance at 0.05 s from 100 to 50 Ω. Figs. 9 and 10 show the DC bus voltage performance and grid current THDs for both control strategies. From this comparative study, it can be observed that the PIC strategy achieves the worst performances in terms of transient time and undershoot rejection ability, while the proposed RBSC strategy has a very small undershoot and transient

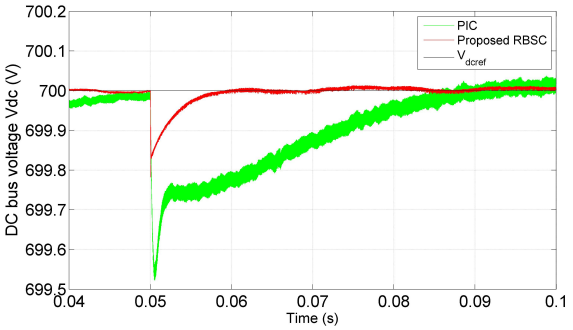

Fig. 9. Comparison of FLVSR DC bus voltage performance with the traditional PIC strategy and the proposed RBSC strategy under load change from 100 to 50 Ω with C_{dc} = 6 µF.

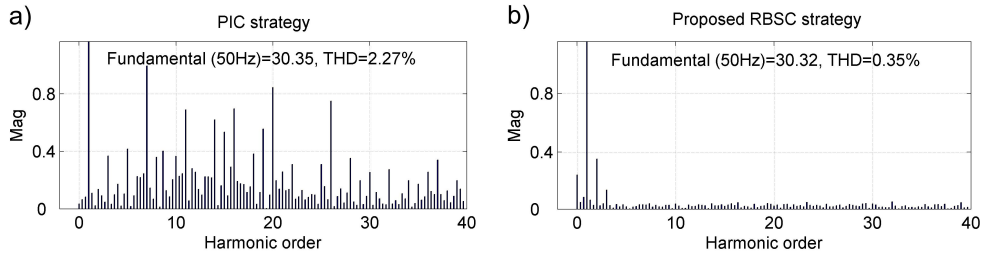

Fig. 10. Grid currents THDs under C_{dc} = 6 µF when the load is changed from 100 to 50 Ω. a) PIC strategy, b) the proposed RBSC strategy.

time, which proves the high robustness of the proposed RBSC against DC capacity and load resistance variations and the high disturbance rejection ability.

Compared to Test 3, when the C_{dc} value is 3 µF, the grid current THDs are increased from 0.31% to 0.35% using the proposed RBSC and from 1.94% to 2.27% using the PIC, as shown in Fig. 10, which again demonstrates the superiority of the proposed RBSC.

In the second scenario of this test, the filter inductance was varied from 1 to 3 mH to evaluate the robustness of both control strategies, as shown in Fig. 11. From this, it can be observed that the THDs are decreased from 1.25% to 0.27% using the proposed RBSC and from 3.39% to 1.4% using the PIC, which also proves the high robustness of the proposed RBSC against filter inductance variations.

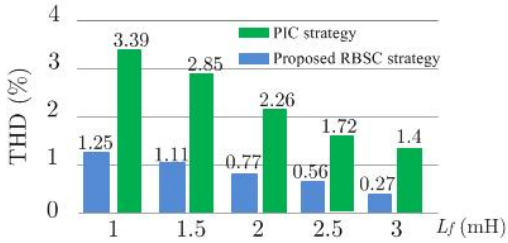

Fig. 11. Comparison of grid currents THDs versus filter inductor variation with the PIC and the proposed RBSC.

5. Conclusions

This paper has proposed a RBSC for a GC-FLVSR with consideration of uncertainties for the task of controlling the DC bus voltage and input currents simultaneously, which leads to high robustness against parametric uncertainties. Moreover, it employs four controllers: including three for the input currents and one for the DC bus voltage. Based on the principle of Lyapunov functions and with consideration of uncertainties, the proposed RBSC strategy can obtain the FLVSR input reference voltages.

The theoretical study and the effectiveness of the proposed control strategy are confirmed using PIL co-simulations using the STM32F407 microcontroller discovery-development-board. Compared to the traditional PIC, the proposed RBSC strategy can obtain lower input current THDs and reduce DC bus voltage ripples with high dynamic response. Thus, it can be observed that the proposed RBSC presents numerous advantages with regard to the linear control strategy, where: the most significant are: sinusoidal currents with high quality; stable DC bus voltage with lower ripples; fast response time; unity power factor; high robustness against parametric variations; easy implementation; ability to enhance the integral DC-bus voltage and input current errors performance indexes. It also offers rather high voltage disturbance rejection ability. Therefore, it is concluded that the proposed RBSC strategy is a more favourable and feasible scheme for grid-connected four leg PWM converters.

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