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Boosting resonant switched-capacitor voltage tripler

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Abstract: This elaboration presents the concept of a unidirectional DC–DC switched-capacitor converter operating as a voltage tripler. The system consists of two resonant cells with switched capacitors and chokes. This proposed converter topology achieves low voltages on semiconductor switches (diodes and transistors) compared to the classic SC series-parallel converter or the boost topology. The output voltage on the capacitors is reduced in the proposed converter because it is divided into two series-connected capacitors with asymmetric distribution. The presented results describe the analytical description of the system operation and the analytical equation for semiconductor currents. A simulation and experimental results have been performed. The system efficiency and three voltage gain values were measured in the experimental setup. The efficiency measured was also compared with the analytical determination curve for loss analysis and further converter optimization.

Key words: boost topology, DC–DC converters, switched-capacitor converter

1. Introduction

Switched-capacitor (SC) systems are often used as DC–DC boost topology [1, 2]. The SC converters are designed to reduce the number or inductance value of power choke. As a result, it allows one to achieve a smaller size and lower weight of the converter system.

Works [3, 4] present the systems that allow obtaining the output voltage twice the value of the input voltage (the voltage doubler), due to the use of series resonance effect, which allows the reduction of losses of switching transistors. Zero current switching (ZCS) leads to noticeably high efficiency (97.0–98.5%). Moreover, these circuits consist of a relatively small number of elements, i.e. two transistors, two diodes, a resonant capacitor, resonant choke and an output capacitor.

Recently, many topologies of the Dickson family have been discussed in [5–8]. Interleaved circuits with switched capacitors can achieve high gain values [5, 7, 8] or work as a voltage lowering circuit [6].

An example of the SC converter allowing one to obtain various voltage gain is presented in [9]. The value of the output voltage depends on the duty cycle of the control pulses. Voltage stresses of the switches are lower than the output voltage [9].

The circuit described in [10] has three voltage outputs with maximum gains equal to two, four and six, respectively. The voltage gain can be smoothly regulated by changing the activation time of one of the transistors [10]. The converter uses four transistors and the maximum voltage of the switches is limited to the input voltage value or twice its value.

The circuits described in [11] and [12] have a voltage gain equal to three. It uses two transistors, the switching losses are limited by the phenomenon of series resonance, which results in soft switching. An important feature of these converters is the common grounding of the input and output voltages.

Boost DC–DC converters are used, among others, in hybrid cars to ensure the appropriate level of input voltage for the motor inverter [13]. In addition, they are used in cars to power lamps [14] and in systems powered by fuel cells or photovoltaic installations [9].

The DC–DC converters with the topology presented in [15–17] are similar to those presented in [3–12], which can also be used as power factor improvement (PFC) circuits. Paper [15] describes a three-level boost converter. The converter [15] operates in the discontinuous conduction mode as a PFC converter with spread spectrum frequency modulation. The proposed control method allows one to reduce electromagnetic interference and increase overall efficiency.

Article [16] describes the three-level DC–DC buck converter of the switched-inductor voltage-lift type. This circuit includes three transistors. Two of them are switched complementary. When the duty cycle of the control signal in the third transistor changes, the circuit voltage gain is adjusted. It is possible to obtain enormous gain values greater than 10, while maintaining low voltage stresses of the transistors. The circuit from [15, 16] also has a modification (replacing the diodes with transistors), which allows two-way energy transfer as in the classic two-level boost circuit [17]. The SC family of converters can control the output voltage [3, 10], similar to the previous converter [15, 16].

The control can be carried out by changing the duty cycle, switching frequency or phase shift of the PWM signals (in the case of systems with more switches).

The proposed converter has a topology close to the automatic interleaved Dickson switched capacitor converter (AIDSCC) described in [5]. An important difference is the way the C_{out2} capacitor is connected. In the proposed system, it is connected between the negative pole of the output voltage and the negative pole of the input voltage (the grounding of the system). In the AIDSCC, it is connected between the negative pole of the output voltage and the positive pole of the input voltage. This topology change has significant implications.

The AIDSCC voltage U_{out2} is $-2U_{\text{in}}$. Therefore, it is necessary to select a capacitor for a voltage value twice as high as that of the considered system. Furthermore, for the AIDSCC circuit, the output voltages U_{out1} and U_{out2} do not have common grounding, as is the case in the proposed circuit. The proposed converter can be used in systems where the input and output common grounding is not required. For this reason, it could be suitable in renewable systems as the front-end DC–DC power conversion, auxiliary power supplies, battery equalizer, and

in automotive applications, as well as in high-intensity discharge lamp supply units in vehicle headlights [10, 17, 18].

The paper is organized as follows. Section II presents the theoretical aspects of the proposed DC–DC converter with an analytical description. Section III contains the results of the simulation described in Section II. Section IV provides laboratory measurements of the proposed system. The waveforms of the voltages and the current of the selected power elements are presented. An efficiency test with voltage gain for a variable load is included in the chart.

2. Concept of the novel converter

2.1. Principle of operation

The proposed converter is shown in Fig. 1. The principle of its operation assumes that the transistors are switched on alternately with a constant 50% duty cycle in the dead time. For analytical considerations, the dead time has been omitted. The complementary switching of the transistors causes the current to flow through the chokes (L_1 and L_2) and the charging capacitors C_1 and C_2 from the input source (Fig. 2). The topology in Fig. 1 can also be extended by many cells, e.g. as in [3, 5, 7, 10–12]. This extension allows one to increase the voltage gain by adding more diodes and capacitors [11] (or capacitors with extra chokes [3, 10]). The modification of the converter assumes that the two chokes are replaced by one L choke.

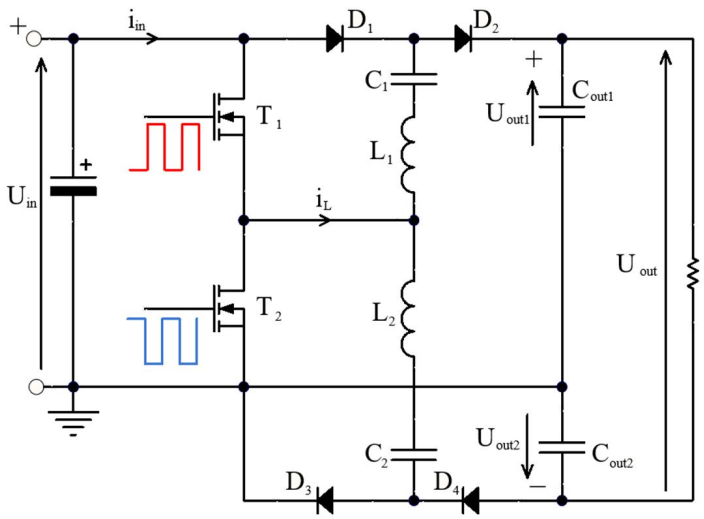

Fig. 1. The novel concept of unidirectional DC–DC high-voltage-gain converter (voltage gain $G = 3$, $G = 2$ or $G = -1$ and the number of switches $s = 2$)

Overcharged capacitors will provide energy for the output capacitors C_{out1} and C_{out2}. The circuit with the D_1 and D_2 diodes together with the C_{out1} capacitor forms a double voltage $(2 - U_{\text{in}})$, while the D_3 and D_4 diodes with the C_{out2} capacitor are the circuit that ensures the

input voltage inversion ($-U_{\text{in}}$). Consequently, the output voltage can be described as:

$$U_{\text{out}} = U_{\text{out1}} - U_{\text{out2}} = 2 \cdot U_{\text{in}} - (-U_{\text{in}}) = 3 \cdot U_{\text{in}} \,. \tag{1}$$

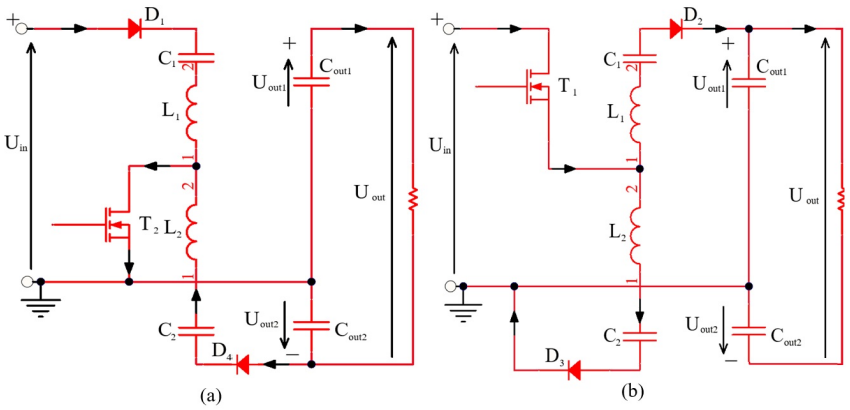

Fig. 2. The operation state: charging (a); discharging (b)

2.2. Input current determination

Figure 3 shows the theoretical waveforms for the proposed control. It should be emphasized that the value of the input current i_{in} indicates the current after the filter capacitor. Operation with a frequency close to the resonant f_0 (L_1 and L_2 with C_1 and C_2 capacitors, respectively) results in a sinusoidal current with the value $I_{\text{in max}}$. In the second half-period, when the transistor

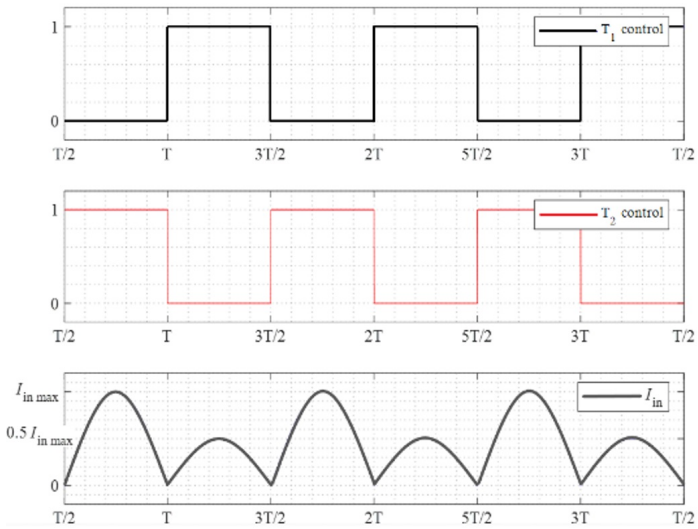

Fig. 3. Theoretical waveforms of the logic signals for transistors T_1 and T_2 with idealized input current

T_1 is turned on, the input voltage and the volt-age on the capacitors are applied to the output capacitors. As a consequence, a current flows through the source with a maximum value twice as low ($I_{\text{in max}}/2$). The average value of the input current can be defined as:

$$I_{\text{in avg}} = \frac{1}{T}\int_0^T i_{\text{in}}(t)\,\mathrm{d}t = \frac{1}{T}\int_0^{T/2} I_{\text{in max}}\sin\omega t\,\mathrm{d}t + \frac{1}{T}\int_{T/2}^{T}\frac{I_{\text{in max}}}{2}\sin(\omega t-\pi)\,\mathrm{d}t. \tag{2}$$

The average value of the input current is:

$$I_{\text{in avg}} = \frac{I_{\text{in max}}}{\pi} + \frac{I_{\text{in max}}}{2\pi} = \frac{3}{2\pi}I_{\text{in max}}\,. \tag{3}$$

The maximum value of the input current is:

$$I_{\text{in max}} = \frac{2\pi}{3}I_{\text{in avg}} = 2\pi I_{\text{out}}\,. \tag{4}$$

2.3. Determination of the current stresses of components

Assuming the ideal half-wave sinusoidal current for diodes and transistors, the RMS current of the switches can be described as:

$$I_{T\,\text{rms}} = I_{T_1\,\text{rms}} = I_{T_2\,\text{rms}}\,. \tag{5}$$

In addition, it can be calculated by:

$$I_{T\,\text{rms}} = \sqrt{\frac{1}{T}\int_0^T i_T^2(t)\,\mathrm{d}t} = \sqrt{\frac{1}{T}\int_0^{T/2}(2\pi I_{\text{out}}\sin\omega t)^2\,\mathrm{d}t} = 2\pi I_{\text{out}}\sqrt{\frac{1}{4}} = \pi I_{\text{out}} = \frac{I_{\text{in max}}}{2}\,. \tag{6}$$

There, the average diode currents for all diodes are equal:

$$I_{D\text{avg}} = I_{D_1\text{avg}} = I_{D_2\text{avg}} = I_{D_3\text{avg}} = I_{D_4\text{avg}}\,, \tag{7}$$

where the mean value is:

$$I_{D\text{avg}} = \frac{1}{T}\int_0^T i_D(t)\,\mathrm{d}t = \frac{1}{T}\int_0^{T/2}\pi I_{\text{out}}\sin\omega t\,\mathrm{d}t = -\frac{1}{2}I_{\text{out}}(\cos\pi-\cos 0) = I_{\text{out}} = \frac{I_{\text{in max}}}{2\pi}\,. \tag{8}$$

The sinusoidal shape of the inductor (and resonant capacitor) current means that the value of the inductor RMS leads to:

$$I_{L\,\text{rms}} = I_{C\,\text{rms}} = \pi\frac{\sqrt{2}}{2}I_{\text{out}} = \frac{\sqrt{2}I_{\text{in max}}}{4}\,. \tag{9}$$

The output capacitor current equals:

$$I_{C\text{out rms}} = \pi I_{\text{out}} - I_{\text{out}}\,. \tag{10}$$

2.4. Voltage stresses of components

The maximum voltage values of the diodes and transistors are approximately equal to the input voltage.

$$U_{D\ \max} = U_{T\ \max} = U_{\text{in}}\,. \tag{11}$$

The mean voltages on resonant capacitors have an approximately constant average value and amount to:

$$U_{C_1\text{avg}} = U_{C_2\text{avg}} = U_{\text{in}}\,. \tag{12}$$

The voltages for the output capacitors are approximately equal to:

$$U_{C\text{out1}} = 2U_{\text{in}}\,, \tag{13}$$

$$U_{C\text{out2}} = -U_{\text{in}}\,, \tag{14}$$

$$U_{C\text{out}} = 3U_{\text{in}}\,. \tag{15}$$

2.5. Efficiency analysis

The converter efficiency equals:

$$\eta \triangleq \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{in}} - \Delta P_C - \Delta P_{\text{SW}} - \Delta P_{Qrr}}{P_{\text{in}}} = 1 - \frac{\Delta P_C + \Delta P_{\text{SW}} + \Delta P_{Qrr}}{P_{\text{in}}}\,, \tag{16}$$

where: ΔP_C represents the conduction losses, ΔP_{SW} represents the switching losses. The turn-off switching losses are practically equal to zero, due to the soft switching (ZCS). However, there is a turn-on switching loss associated with charging and discharging the output capacitances of the FETs [20]. The total switching power losses ΔP_{SW} are equal only to the losses E_{on}:

$$\Delta P_{\text{on}} = \sum_{l=1}^{2} E_{\text{on}l} f_S\,. \tag{17}$$

The total conduction losses are the sum of the conduction loss ΔP_T in the transistors, the loss ΔP_D in the diodes, and the loss ΔP_L in inductance:

$$\begin{aligned}\Delta P_C = \Delta P_T + \Delta P_D + \Delta P_L + \Delta P_C = \sum_{k=1}^{2} R_{DS(\text{on})k} I_{Tk}^2 + \sum_{l=1}^{4} V_{Fl} I_{Dl\text{avg}} \\ + \sum_{z=1}^{2} R_{L\text{-ESR}} I_{Lz}^2 + \sum_{z=1}^{2} R_{C\text{-ESR}} I_{Lz}^2 + \sum_{z=1}^{2} R_{C\text{out-ESR}} \left(I_{C\text{out rms}}\right)^2\,,\end{aligned} \tag{18}$$

where: $R_{DS(\text{on})}$ is the MOSFET turn-on resistance, V_{Fl} is the diode voltage drop, R_{AC} is the inductor equivalent resistance (measured by an impedance analyzer for an operating frequency of 100 kHz), $R_{C\text{-ESR}}$ is the resonant capacitor equivalent resistance, $R_{C\text{out-ESR}}$ is the output capacitor equivalent resistance. The turn-off power loss generated by the switching diode ΔP_{Qrr} is:

$$\Delta P_{Qrr} = \sum_{l=1}^{4} f_S V Q_{rrl}\,, \tag{19}$$

where V is the diode blocking voltage and Q_{rr} is the diode reverse recovery charge. The overall efficiency equals:

$$\eta_{T\,\mathrm{OSCVM}} = 1 - \frac{\left[\pi^2 \left(R_{L\text{-ESR}} + R_{C\text{-ESR}}\right) I_{\mathrm{out}} + 2R_{C\mathrm{out\text{-}ESR}} \left(\pi I_{\mathrm{out}} - I_{\mathrm{out}}\right)^2\right]}{P_{\mathrm{in}}} - \frac{2\pi^2 R_{DS(\mathrm{on})k} I_{\mathrm{out}}^2 + 4V_{Fl} I_{\mathrm{out}}}{P_{\mathrm{in}}} - \frac{2f_S(2U_{\mathrm{in}}Q_{rr} + E_{\mathrm{on}})}{P_{\mathrm{in}}}. \tag{20}$$

3. Simulation results

3.1. Steady state operation

The results in Fig. 4 show only the steady state operation simulation of the power converter (simulation parameters are listed in Table 1). Key values for voltage or current have been defined for chokes, capacitors, and semiconductor elements. The simulation results confirmed (Fig. 4) that both transistors have a similar RMS current value, and the voltage across the transistors is equal to the input voltage. The simulation results obtained are approximately consistent with the theoretical runs. The current waveforms differ to some extent from the expected ones because of the inconsistency of the elements (e.g. the conduction resistance of transistors and voltage drops on the diodes).

Table 1. Parameters of the converter and input voltage for the simulation model

Parameter name	Symbol	Value	Unit
Inductance	L_1, L_2	1.7	µH
Capacitance	C_1, C_2	1.1	µF
Resistance drain-source	$R_{DS(\mathrm{on})}$	80	mΩ
Diodes 1–4 forward voltage	V_F	0.5	V
Input voltage	U_{in}	100	V
Switching frequency	f_s	100	kHz

The system analysis shows that semiconductor elements have identical current loads and voltage stresses, which is a great advantage of the system. Resonance capacitors also have the same voltage with the same effective value.

For the same parameters (Table 1) of the simulation system, the gain values were tested at different outputs of the system (Table 2).

The values of the load resistances from Table 2 have been selected, so that the output current is approximately 1 A. The load of one of the outputs has a relatively small influence on the values of the gains. In the case of no load, the voltages of the output capacitors increase significantly. The values of these voltages are limited by losses in the system.

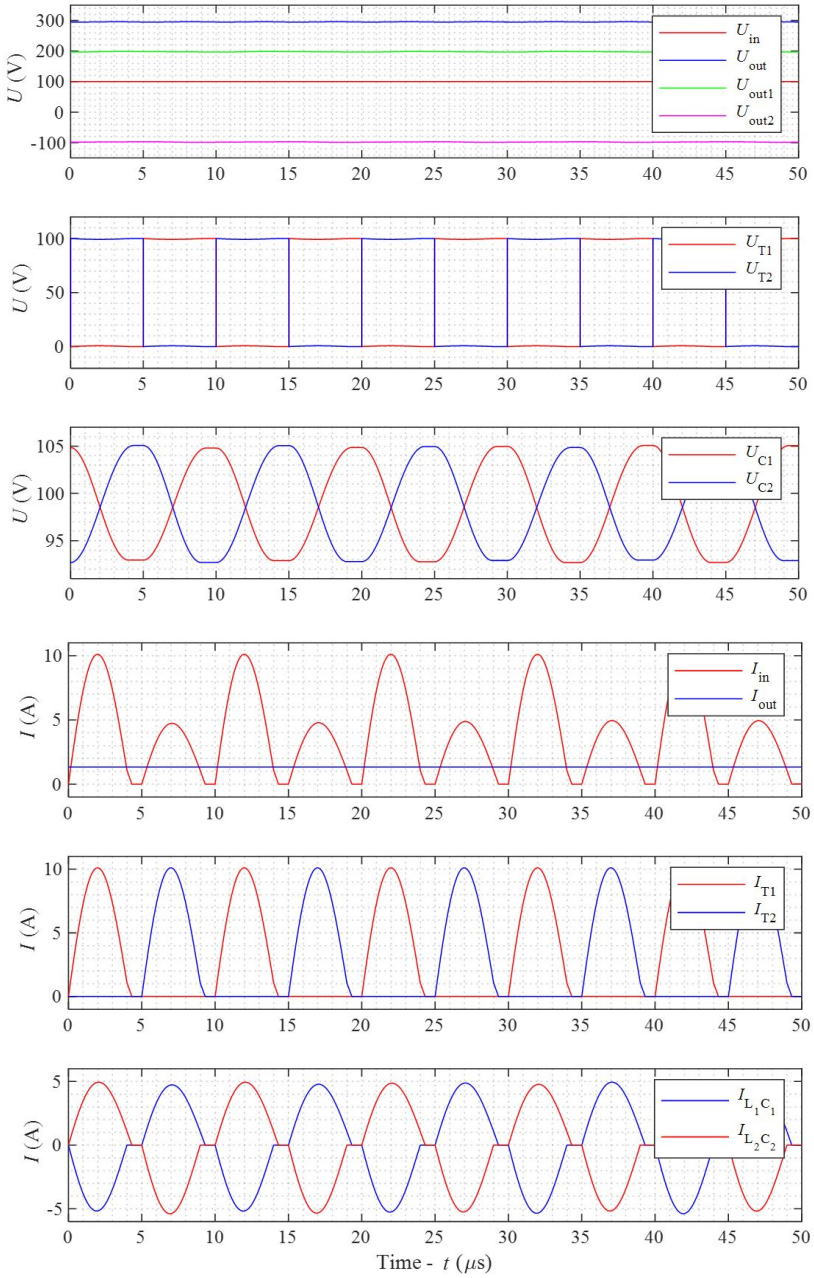

Fig. 4. Waveforms of voltages (input, output and capacitors) and currents (input, output, transistors and *LC* branches) of proposed converter operating. Matlab/Simulink results for 400 W of output power (U_{in} = 100 V and f = 100 kHz)

Table 2. Simulation results (input voltage 100 V and frequency 100 kHz)

Parameters	$\boldsymbol{R_1 = 200\ \Omega}$ $\boldsymbol{R_2 = \infty}$ $\boldsymbol{R = \infty}$	$\boldsymbol{R_1 = \infty}$ $\boldsymbol{R_2 = 100\ \Omega}$ $\boldsymbol{R = \infty}$	$\boldsymbol{R_1 = \infty}$ $\boldsymbol{R_2 = \infty}$ $\boldsymbol{R = 300\ \Omega}$	$\boldsymbol{R_1 = 200\ \Omega}$ $\boldsymbol{R_2 = 100\ \Omega}$ $\boldsymbol{R = 300\ \Omega}$	$\boldsymbol{R_1 = \infty}$ $\boldsymbol{R_2 = \infty}$ $\boldsymbol{R = \infty}$
G_1	1.99	2.07	1.97	1.95	2.53
G_2	–1.07	–0.99	–0.97	–0.95	–1.50
$G = G_1 - G_2$	3.06	3.06	2.94	2.91	4.03

4. Experimental results

4.1. Experimental setup

The proposed DC–DC converter was experimentally investigated to verify the operation principle, switching concepts, voltage gain, voltage stresses on switches, power losses, efficiency, and temperature field distribution. Table 3 sums up the major converter (Fig. 5) parameters and

Table 3. Parameters of the laboratory setup

Parameter	**Value**
Input voltage U_{in}	100 V
Input capacitor	EPCOS electrolytic 50 µF ±20% with MKP 4.7 µF ±5% and MKP 1 µF ±5%
Output capacitor C_{out1} and C_{out2}	4.7 µF ±5% (MKP capacitor) $R_{C\text{out–ESR}}$ = 5.8 mΩ
SC capacitance C_1 and C_2	1100 nF, $R_{C\text{-ESR}}$ = 2.6 mΩ
Inductor – L_1 and L_2	1.7 µH
Inductors R_{DC} (DCR) and R_{AC}	R_{DC} = 1.4 mΩ R_{AC} = 115.1 mΩ for 100 kHz
Resonant frequency	$f_0 \approx$ 116.4 kHz
Operating frequency	$f_S \approx$ 00 kHz
SiC MOSFET transistors	C3M0060065D (V_{DS} = 650 V, I_D = 29 A, $R_{DS(\text{on})}$ = 60 mΩ)
Single-channel driver for high side and low side	1EDI60H12AH – 6.0 A high-side isolated gate driver
Isolated DC–DC supply for driver	MGJ2D051505SC (P = 2 W, U_{input} = 5 V, U_{input} = +15 V/–5 V)
Diodes	VB60170G-E3 (I_F = 2 × 30 A, V_{RRM} = 170 V, V_F = 0.65 V at 5 A, 25°C)
PWM generator	External board DE10-lite Control Board
Dead time	50 ns

laboratory setup for the experiment. The prototyping half bridge (Fig. 5(a)) was used to check only the topology operation. The volume and efficiency optimization were not the main goals of the article.

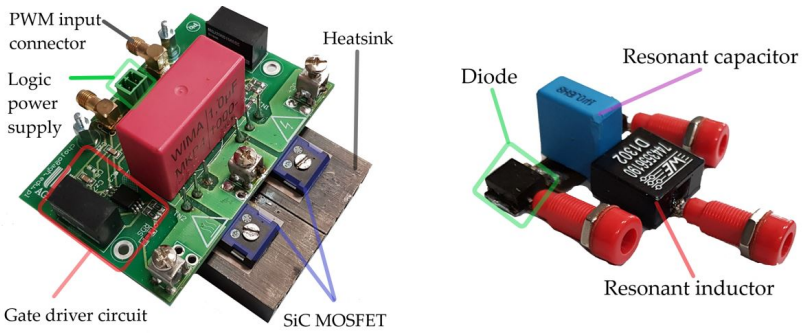

Fig. 5. Experimental board: half bridge (a); with resonant *LC* circuit diodes (b)

4.2. Operation of the converter

The subsection presents the results for the steady state. The Tektronix TCP0030A current probe with a 120 MHz band [21] was attached to the MDO3000 series oscilloscope [22], and passive TPP1000 probes (CAT II up to 300 V) with a 1 GHz band were used to measure the voltage in the components [23]. The results of the measurement of the input voltage and possible output voltages are shown in Fig. 6.

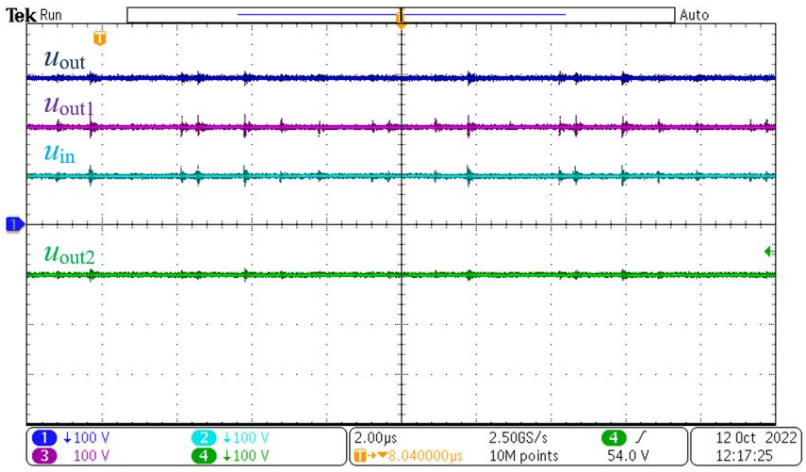

Fig. 6. Experimental waveforms of the converter for $P_{in} \approx 400$ W and $U_{in} = 100$ V – output voltage u_{out} (CH1), input voltage u_{in} (CH2), first output voltage with $G = 2u_{out1}$ (CH3) and second output voltage with $G = -1u_{out2}$ (CH4s)

The results of the choke current measurement i_L ($i_{L1} + i_{L2}$) and the voltages of the resonant capacitor C_1 are shown in Fig. 7. The results are similar to the simulation results in Fig. 4. The voltage waveforms for transistors (with resonant inductor current) and diodes are shown in Fig. 8 and Fig. 9, respectively. In a steady state, the voltage value is close to the input voltage ($U_{\text{in}} \approx 100$ V). The visible overshoot is the result of parasitic inductance in the power circuit.

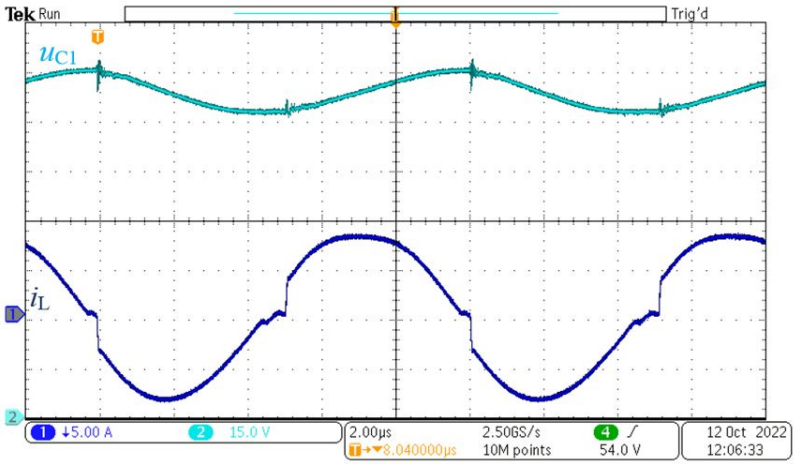

Fig. 7. Experimental waveforms of the converter for $P_{\text{in}} \approx 400$ W and $U_{\text{in}} = 100$ V – resonant inductor ($i_L = i_{L1} + i_{L2}$) current (CH1) and voltages across resonant capacitor C_1 (CH2)

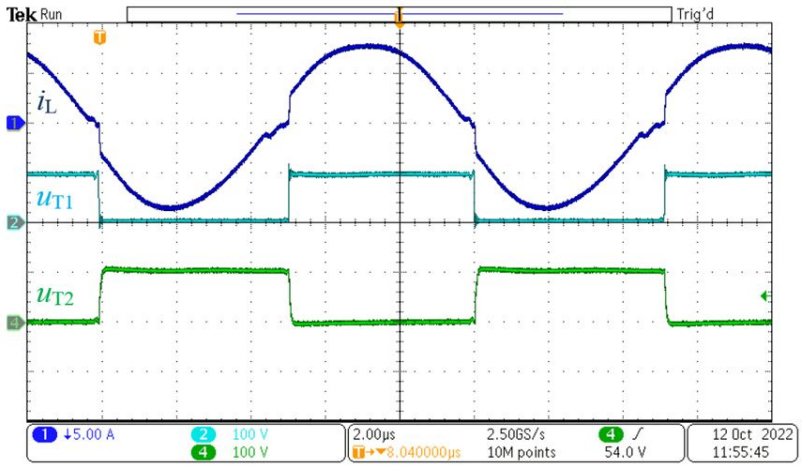

Fig. 8. Experimental waveforms of the converter for $P_{\text{in}} \approx 400$ W and $U_{\text{in}} = 100$ V – resonant inductor ($i_L = i_{L1} + i_{L2}$) current (CH1) and voltages across transistors T_1 (CH2) and T_2 (CH4)

Figure 10 shows the result of the thermography of the converter operating at a power of $P_{\text{out}} \approx 375$ W. These results show that the heat dissipation in switches and diodes is not significant.

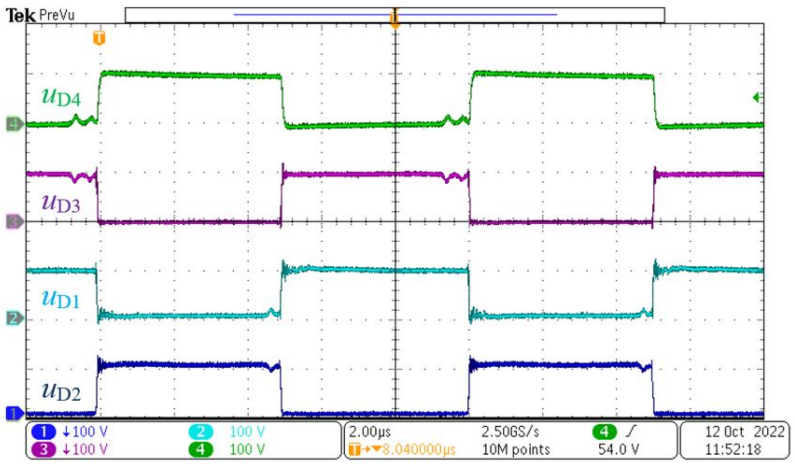

Fig. 9. Experimental waveforms of the converter for $P_{\text{in}} \approx 400$ W and $U_{\text{in}} = 100$ V – voltages across diodes D_2 (CH1), D_1 (CH2), D_3 (CH3) and D_4 (CH4)

However, you can observe a concentration of heat near the resonance coil. The L_1 choke (+69.5°C) is the hottest point in the power circuit. The high temperature is caused by the lack of an active cooling system.

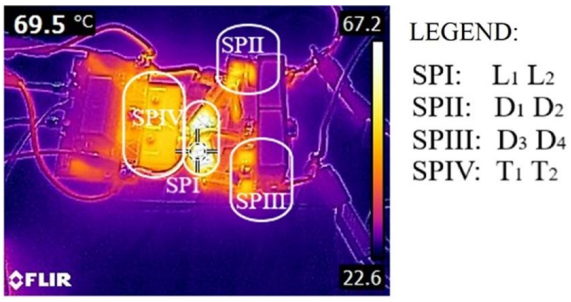

Fig. 10. An infrared photo of the converter during constant operation for 600 W – transistors with heat-sink and no forced air flow

4.3. Efficiency and voltage gain

Figure 11 shows the graph of efficiency vs the output power function. A series of measurements were performed at a constant switching frequency of $f_S = 110$ kHz. Efficiency was measured using a Yokogawa WT 1500 power analyzer [24]. The maximum efficiency of the converter was equal to $\eta_{\max} = 97.29\%$.

The curve plotted on the basis of the results from Eq. (20) for the parameters in Table 3 was added to the results. The equivalent resistance value for a choke was determined by the impedance analyzer $R_{AC} = 115.1$ mΩ [25]. Other parameters are specified in the technical doc-

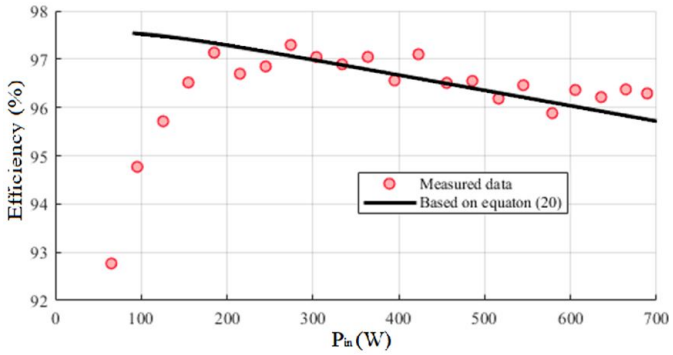

Fig. 11. Efficiency vs output power (U_{in} = 100 V and $f_S \approx$ 100 kHz)

umentation [26, 27]: the transistor resistance $R_{DS(\text{on})\,\text{max}}$ = 80 mΩ, C_{oss} stored energy E_{oss} 1 µJ for 100 V (marked with dashed line in Fig. 11) and the turn-on energy were calculated based on the current value (Fig. 12) and diode forward voltage V_F = 0.65 V.

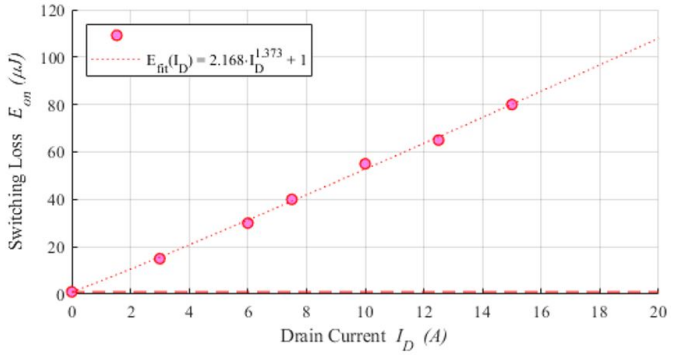

Fig. 12. Turn-on losses vs drain current for 100 V and V_{GS} = −4 V/+5 V

The analytical curve describing the losses in the proposed converter allows one to determine the percentage of loss for each of the components (Fig. 13). The losses are mainly caused by the conduction resistances of the MOSFETs (37% for 350 W) and the diode forward losses (27% for 350 W). Transistor conduction losses and inductor losses (R_{AC} equivalent resistance) are significant for high load (700 W). The summarized capacitors conduction losses have a slight effect on overall efficiency (< 2%). Based on Fig. 13, the direction of optimization of the system can be determined. The diode turn-off power losses ΔP_{Qrr} were assumed neglected because there was not information on the Q_{rr} recovery charge in datasheet [25].

Figure 14 shows the measured voltage gains as a function of the output power (in the range from 50 to 375 W) – the voltage variation (for all possible outputs) can be determined by a linear relationship.

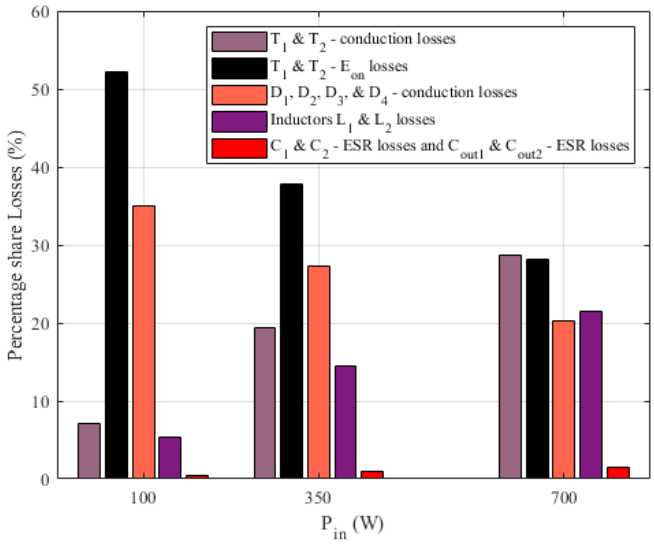

Fig. 13. Losses analysis of the converter for 100 W, 350 W and maximum input power 700 W

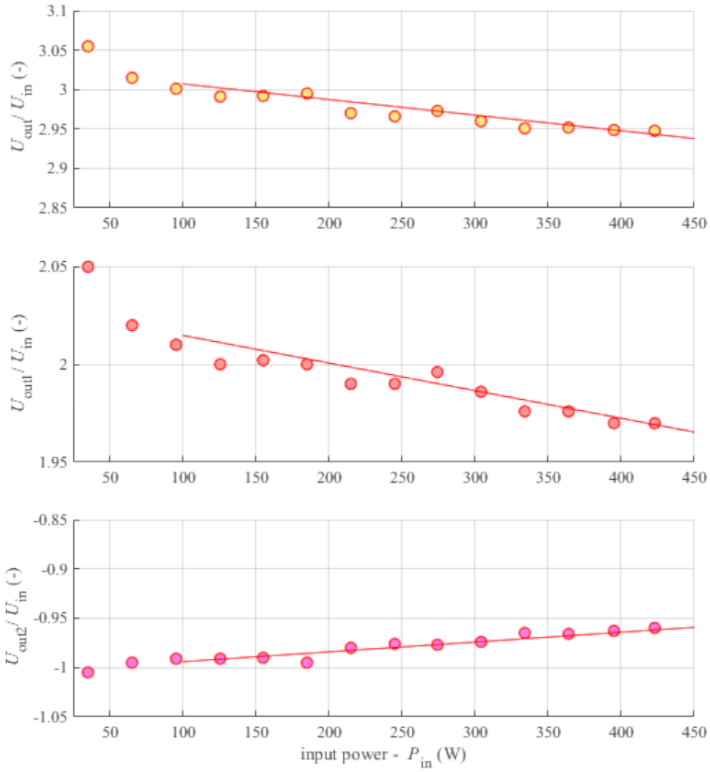

Fig. 14. Voltage gain vs output load (U_{in} = 100 V and $f_S \approx$ 100 kHz)

4.4. Output voltage control

There is a possibility to control output voltages by changing the duty cycle of transistors control signals. However, only for the value of a duty cycle near to 50%, operating with zero current switching is possible. Different duty cycle values will result in the transistor turning-off while charging or discharging switched capacitors. This will result in hard turn-off and increase switching losses (no ZCS during turn-off transient process).

There are two ways of changing the duty cycle. The first is reducing the duty cycle value for both transistors, maintaining a shift in time equal to half of the switching period. The second way is reducing (or alternatively increasing) the duty cycle for transistor T_1, and controlling transistor T_2 is the negation of the former. In both options, the gain vs duty cycle characteristic is similar.

Figure 15 shows the relation between the voltage gains and duty cycle for the first way of changing the duty cycle. For a duty cycle near to zero, G_1 is close to 1, G_2 is close to zero and as a consequence G is approximately equal to 1. The absolute values of gains are growing nonlinearly with an increase in duty cycles.

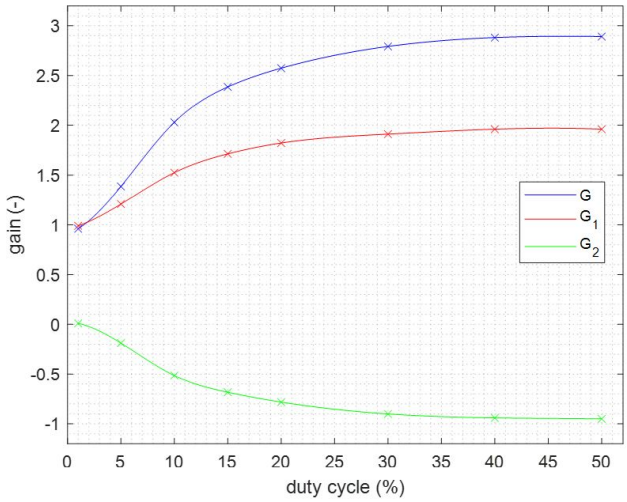

Fig. 15. Gain vs T_1 duty cycle (T_2 control is a negation of T_1 control) for 300 W for resistive load 220 Ω (U_{in} = 100 V and f_S = 100 kHz)

5. Conclusions

This paper presents a general-concept topology and switching methods of the proposed DC–DC converter. The research results presented in this paper confirm that the proposed converter contains various superior qualities, such as the following:

– Three possible voltage gains. The theoretical maximum voltage gain of the converter can reach three $G = 3$ but it can also provide $G = 2/-1$ with common grounding,
– Low number of switches. The converter requires only two switches and four diodes, which is favorable compared to different SC converters such as in [10] or [17],

– The principle of operation assumes the transfer of energy through the capacitors. A tiny choke has been used to achieve a quasi-sinusoidal current in the circuits where the switched capacitors are charged and discharged,
– Low voltage stresses on switches and diodes. All elements' voltage stress is equal to input voltage (beside voltage overshoot),
– The efficiency was greater than 96% in the range from 120 W to 500 W (with the highest value $\eta_{\max} = 97.29\%$). Furthermore, the design can be improved with a focus on minimizing resistances.

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