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OTA Based Mem-capacitor Validation and Implementation Using Commercially Available IC

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***Abstract*—This paper discusses a mem-capacitor circuit which is based on two MO-OTA along with a multiplier and 4 passive elements. This circuit is a charge-controlled memcapacitor emulator which is independent of any memristor also it consists the feature of electronic tunability. Additionally, this circuit is simpler and uses less hardware because it lacks a mutator and uses fewer active-passive components. The circuit behaviour is justified through various simulations in cadence Orcad tool with 180nm CMOS TSMC parameters. Additionally, conclusions from simulations and theory are validated experimentally through commercially available IC.**

***Keywords*—Memcapacitor; memristor; transconductance; mutator; tunable; hysteresis**

I. INTRODUCTION

MEM-ELEMENTS (Memristor, Memcapacitor, and Meminductor) are nonvolatile nanoscale memory devices without an external power source. They are consequently considered to be a component of analog signal processing that is still evolving. L. Chua was the first to present the memristor as a fourth circuit component in his research papers that were published in 1971 and 1976 [1]-[2], in which a mathematical relationship was established between the basic circuit variables. In 2009[3], Ventra created an enlarged memristor (MR) theory that also includes memcapacitor (MC) and meminductor (MI), which at the time was not well-known. The Hewlett Packard research team claimed to have an experimental memristor in 2008 [4]. The relationship between the circuit elements of a memory device, which may become more nonlinear or linear when lower or higher frequencies are applied, respectively, results in a constricted hysteresis loop. A restricted hysteresis loop can be used to visualise the voltage-charge relationship in a memcapacitor [5].

The literature has documented numerous uses for memcapacitors, including memory devices, chaotic circuits, oscillators, etc. [6]-[7]. Some mathematical and PSPICE models based on MC emulator have also been presented in the literature [8]-[9]. In the literature that is currently available, active and passive component-based MCs are reported in Refs. [10–25], which may be further classified as MC emulators without MR [10],[12]–[13],[17]–[19],[22],[24]–[25] and MR-based emulators, also known as mutator approach [11,14–16,20–21,23].

It has been discovered that the MC emulator without MR works well for frequency selection, compatibility, and matching problems. Only a few MC emulators [10], [13], [18]-[19], [24] are determined to be good in the MC design in terms of compatible numbers of active components (three [10], three [13], four [18], three [19], and five [24]) and passive elements (2-C, 3/5-R [7], 2-C, 2-R [13], 2-C, 1-R [18], 3-C, 1-R [19], and 3-C,2-R [24]).

In addition, other two MC emulators were developed utilising either a varactor diode [17] or an LDR (Light Depending Resistor) [12]. The LDR constrains the frequency ranges (0.1 Hz to 10 Hz) and running speed of the circuit, while the Varactor diode needs an additional power source to work in the reverse bias. Another MC emulation in Ref. [22] uses five active elements and none passive element, however, the device uses its own intrinsic (parasitic) capacitor as a passive element, limiting its frequency for lower range since parasitic effects can be seen at higher frequency. J. Vista also provided a new design based on the DXCCDITA active element [25], but the article did not provide any experimental data from the MC emulation.

Moreover, MC emulator based on MR mutator approach are detailed in Refs. [11], [14]-[16], [20]-[21], [23] in which More specifically, Y.V. Persin [11] suggested MC and MI emulator utilising a digital potentiometer manufactured by programmable (continuous update in resistance) using microcontroller. B. Biolek [14] also provided a slight adjustment to the scheme for converting MR to MC after taking the parasitic effects into account. However, this method works well for creating discrete circuit components but not integrated circuits. Yu et al [15], Shah et al [16], Z. Taskıran et.al [23] have presented different mutator-based approaches. Due to its novel technique of having no grounded limits, MC emulator in Ref. [15] is deemed popular. However, for implementation, all three emulators use a greater proportion of active elements (2-OP-AMP, 4-AD-844, 1-Multiplier [15], 2-CCII, 3-OP-AMP, 1-Multiplier [16], and 2 CBTA, 1-Multiplier [23]) as well as passive components (2-C, 9-R [15], 2-C, 4-R [16], and 2-C, 2-R. Other circuits in References [20]–[21] include numerous active and passive components and have configurable features, although these have a constrained operating frequency range. However, frequency selection, compatibility, and matching issues may also arise when using the mutator technique, which converts MR nonlinear qualities into MC characteristics.

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This paper presented a mathematical validation of memcapacitor circuit of Ref. [13]. In addition the circuit simulation are also carried out and verified through experimental setup using commercially available ICs. The design is easier and uses a novel MC emulator without any MR mutator. The simulations are done in cadence Orcad tool with 180nm CMOS TSMC parameters. .After all, the proposed design behaviour observed by both simulation and experimental results shows the good agreement with the available circuits.

II. MEMCAPACITOR THEORY AND METHODOLOGY

In today's life we know only three basic electrical elements resistor, capacitor, and inductor. These are derived from four fundamental circuit variables such as voltage *v*, current *i*, flux ϕ and charge q which results in five well known possible combinations. One more relation can also be established between q and ϕ which is undefined. L. Chua in 1971 [1] proposed a new missing element named memristor and later its other family elements (memcapacitor, mem-inductor) in which a new relationship between charge and flux was established. Out of these, memcapacitor gained a lot of popularity, and many researchers are working in this domain. A charge-controlled memcapacitor relation is given in Eq. (1):

$$v(t) = D_M(\sigma)q(t),\ D_M(\sigma) = \frac{d\phi}{d\sigma} \qquad (1)$$

$$\text{Where, } \sigma(t) = \int q(t)dt,\ D_M = C_M^{-1})$$

where C_m= mem-capacitor, and D_m= inverse mem-capacitor. In this work, a novel electronically tunable emulator for charge-controlled mem-capacitors is presented, utilizing MO-OTAs. The circuit comprises two MO-OTAs, two grounded capacitors, a grounded resistor, a floating resistor, and an analog multiplier as shown in Fig.1.

Figure 2 displays the circuit symbol for the MO-OTA and the terminal relation of MO-OTA described in Eq. (2):

$$I_{ZPi} = -I_{ZNi} = g_m(V_P - V_N) \qquad (2)$$

where g_m is the transconductance value of MO-OTA.

III. MATHEMATICAL ANALYSIS OF CIRCUIT

In this emulator circuit, the charge can be given by:

$$q(t) = \int I_{in}(t).dt \qquad (3)$$

Also, I_{R2} is the current across resistance R_2, it can be given by:

$$I_{R2} = -I_{ZP} = -g_{m2}(V_P - V_N) = \frac{(V_{in} - V_N)}{R_2} \qquad (4)$$

$$\Longrightarrow -g_{m2}R_2V_P + g_{m2}R_2V_N = V_{in} - V_N$$

On solving we get:

$$V_N(1 + g_{m2}R_2) = V_{in} + g_{m2}R_2V_P$$

$$V_N = \frac{1}{1+g_{m2}R_2}V_{in} + \frac{g_{m2}R_2}{1+g_{m2}R_2}V_P \qquad (5)$$

The voltage V_M is obtained by multiplying V_{R1} and V_{C1}, which is expressed in Equation (6). V_{R1} and V_{C1} refer to the voltages across resistor R1 and capacitor C1, respectively. The non-linear characteristics of the emulator are achieved by multiplying the voltages across the capacitor and resistor. Thus voltage across multiplier:

$$V_M = V_{R1} * V_{C1}$$

$$V_{R1} = I_{ZN2} * R_1,\ V_{C1} = \frac{q_{C1}}{C_1} \quad and \quad I_{C1} = -I_{ZN2} = I_{ZP2}$$

$$V_M = -\frac{I_{C1}R_1q_{C1}}{C_1} \qquad (6)$$

Current across Capacitor (C_1):

$$I_{C1} = g_{m1}(V_{P0} - V_{N0}) \qquad \{\therefore V_{P0} = V_{in}\}$$

$$I_{C1} = g_{m1}(V_{in} - V_M) \qquad \{\therefore V_{N0} = V_M\}$$

From equation (6), we get

$$I_{C1} = g_{m1}\left(V_{in} + \frac{I_{C1}R_1q_{C1}}{C_1}\right)$$

$$I_{C1}\left(1 - \frac{g_{m1}R_1q_{C1}}{C_1}\right) = g_{m1}V_{in}$$

$$I_{C1} = \frac{g_{m1}V_{in}}{1-g_{m1}R_1\frac{q_{C1}}{C_1}} \qquad (7)$$

KCL at node 1:

$$I_{in} + I_{ZN1} + I_{ZP} = 0$$

$$I_{in} = -I_{ZN1} - I_{ZP}$$

$$I_{in} = I_{C1} - g_{m2}(V_P - V_N)$$

From equation (5) & (7), we get

$$I_{in} = \frac{g_{m1}V_{in}}{1-g_{m1}R_1\frac{q_{C1}}{C_1}} - g_{m2}\left(V_P - \frac{V_{in}}{1+g_{m2}R_2} - \frac{g_{m2}R_2}{1+g_{m2}R_2}V_P\right)$$

$$I_{in} = \frac{g_{m1}V_{in}}{1-g_{m1}R_1\frac{q_{C1}}{C_1}} - g_{m2}\left(\frac{1}{1+g_{m2}R_2}V_p - \frac{1}{1+g_{m2}R_2}V_{in}\right)$$

$$I_{in} = \frac{g_{m1}V_{in}}{1-g_{m1}R_1\frac{q_{C1}}{C_1}} + \frac{g_{m2}V_{in}}{1+g_{m2}R_2} - \frac{g_{m2}V_P}{1+g_{m2}R_2} \qquad \{\therefore V_P = V_{C2}\}$$

$$I_{in} = \left(\frac{1}{\left(\frac{1}{g_{m1}} - \frac{R_1q_{C1}}{C_1}\right)} + \frac{1}{\left(\frac{1}{g_{m2}}+R_2\right)}\right)V_{in} - \left(\frac{1}{\frac{1}{g_{m2}}+R_2}\right)V_{C2} \qquad (8)$$

From Eq. (3) and (8), q(t) can be obtained as:

$$q(t) = \int I_{in}(t).dt = \left(\frac{1}{\left(\frac{1}{g_{m1}} - \frac{R_1q_{C1}}{C_1}\right)} + \frac{1}{\left(\frac{1}{g_{m2}}+R_2\right)}\right)\int V_{in}(t).dt - \left(\frac{1}{\left(\frac{1}{g_{m2}}+R_2\right)}\right)\int V_{C2}(t).dt \qquad (9)$$

IV. SIMULATION AND EXPERIMENTAL RESULTS

The hysteresis behaviour is observed between charge and voltage in memcapacitor when a sinusoidal voltage is applied at the input. The circuit shown in Fig.1 is designed with the passive components of values R1=800 Ω, R2=10 kΩ, C1=0.1μF, and C2=30μF. The applied sinusoidal input voltage 50mV and

frequency of 200 Hz. Fig. 3(a) shows a hysteresis curve of charge versus voltage and Fig. 3(b) shows the time responses of memcapacitor emulator circuit. To examine the memory feature (non-volatile behaviour) of the proposed mem-capacitor emulator, positive and negative pulses are employed, and the changes in the memcapacitor charge are depicted in Fig. 4. The input voltage amplitude of 50mV and pulse period, pulse on width have been set to 300µsec and 80µsec, respectively. As shown in the figure, the charge of the memcapacitor emulator begins with the value from the previous pulse in each subsequent pulse. This observation confirms both the incremental and decremental existence of the memory feature in the mem-capacitor circuit.

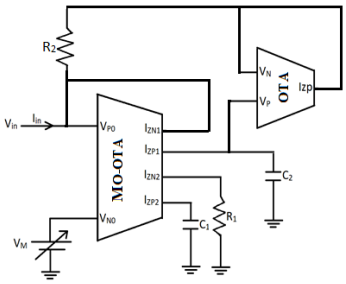


Fig. 1. Memcapacitor emulator based on MO-OTA

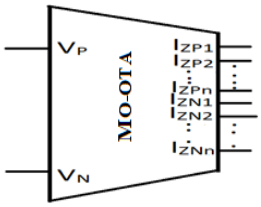
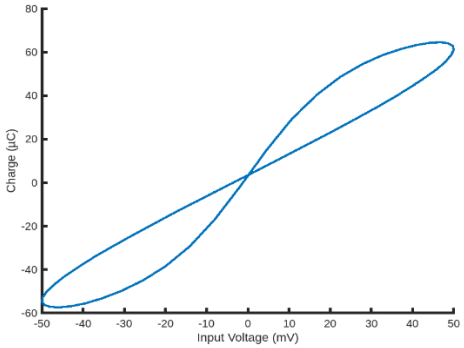
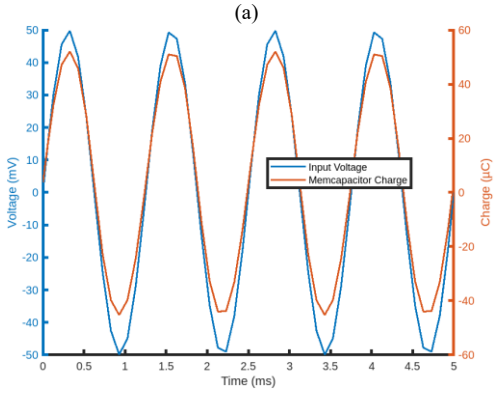


Fig. 2. Circuit symbol of MO-OTA



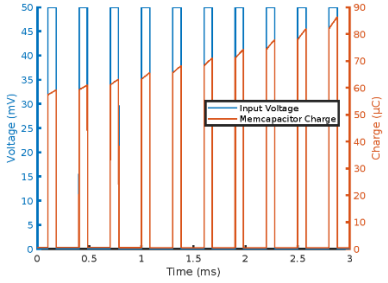
(a)



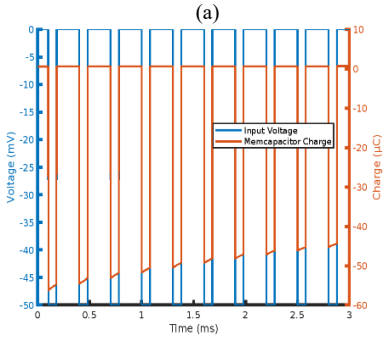
(b)

Fig. 3. (a) hysteresis curve shows voltage-charge relationship (b) input voltage-time and charge-time graph of the memcapacitor.

The electronic tunability of circuit is proven by changing the transconductance value through varying the biasing current of the OTAs form 60µA, 80µA, 100µA, and 120µA as shown in Fig. 5a. Moreover, the memcapacitor circuit is subjected to an input signal voltage of 50 mV over a range of different frequency values. The voltage-charge hysteresis for frequencies of 200Hz, 500 Hz, 800 Hz, 1 kHz and 2 kHz are demonstrated in Fig. 5b, which exhibit a desired characteristics as hysteresis tends towards linearity with the frequency increase. Furthermore, voltage-charge hysteresis for varying amplitudes of input voltages as 20 mV, 50 mV, 100 mV, and 150 mV are also given in Fig. 5c.



(a)



(b)

Fig. 4. Variation of the memcapacitor charge for negative pulses.

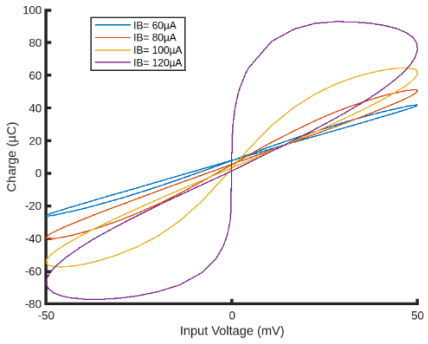


Fig. 5 (a)

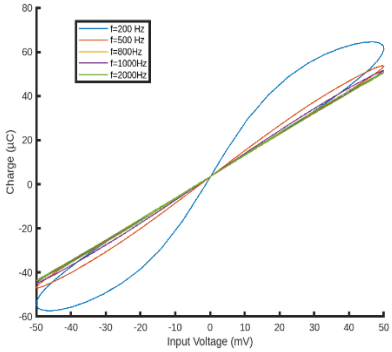
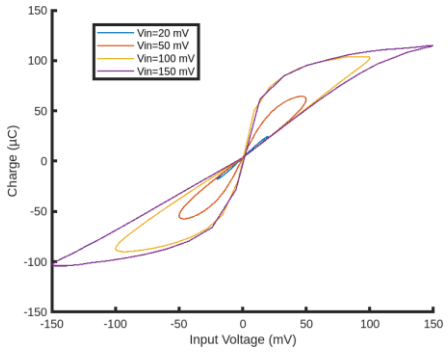


Fig. 5 (b)



(c)

Fig. 5. Input voltage-charge relationship (a) for different biasing current (b) for different frequencies (c) for different amplitudes of input voltage.

The proposed memcapacitor emulator circuit is also verified using commercial available OTA IC CA3080. The implementation of the circuit involves the usage of five CA3080 ICs and an analog multiplier AD633 IC as shown in Fig. 6. In this arrangement a supply voltage of 12Vpp and an input signal of 300 mV peak with frequencies of 50 Hz, 75 Hz and 100 Hz are given to the circuit. The obtained output time domain signal waveform and hysteresis are depicted in the Fig. 7a, 7b, 7c and 7d respectively.

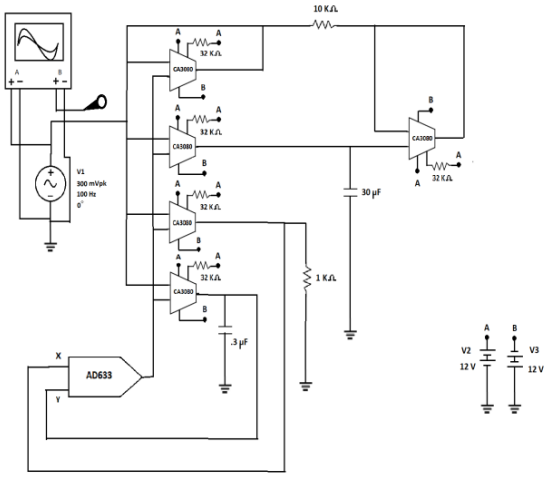


Fig. 6. Circuit diagram for proposed memcapacitor emulator in Multisim

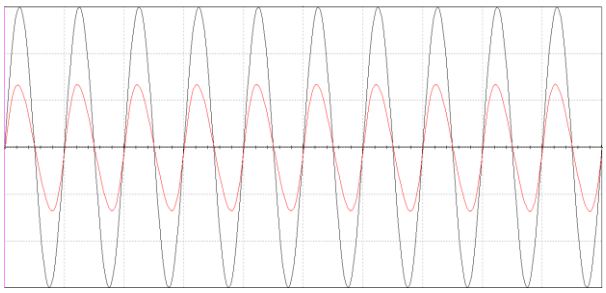
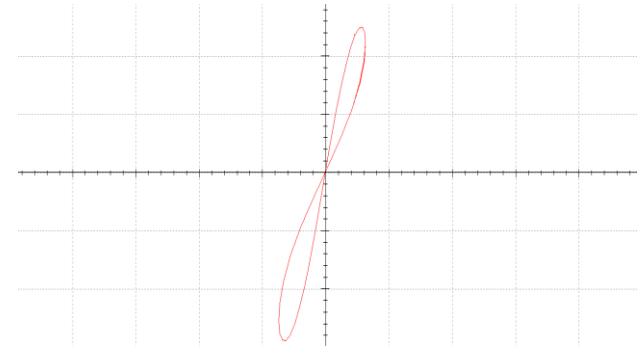
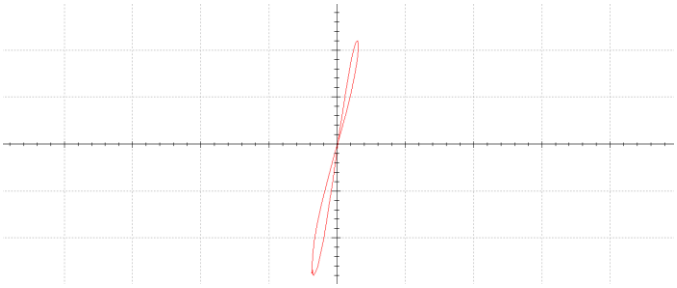


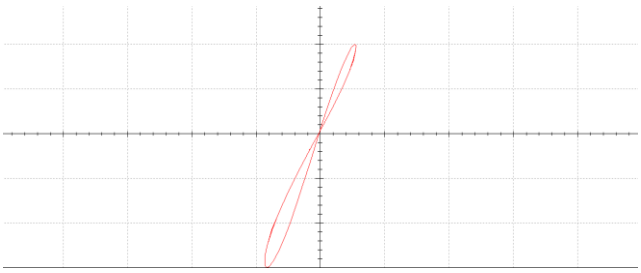
Fig. 7(a).



(b)



(c)



(d)

Fig. 7. (a) Input and output signal waveform in time domain (b) Output hysteresis at 50 Hz (c) Output hysteresis at 75 Hz and (d) Output hysteresis at 100 Hz

CONCLUSION

This study suggests a simple memcapacitor emulator circuit without the requirement for a memristor mutator approach. It is also possible to electronically modify the suggested memcapacitor emulator. The circuit is constructed with the fewest active and passive parts possible. The validity of the circuit is verified using a variety of simulation findings, such as the hysteresis curve of frequency change, input bias variations, input voltage variation, and non-volatile behaviour. Additionally, experimental data for the hysteresis curve are provided, and a hardware model of the suggested memcapacitor emulator is built up using ICs that are easily available on the market. Since the capacitive behaviour of the circuit is independent of the typical requirement of a Mutator, the circuit structure is simpler than the memcapacitor described in literature.

Finally, a summary of memcapacitors available in literature are given in Table I.

TABLE I
SUMMARY OF MEMCAPACITORS AVAILABLE IN LITERATURE

Refs.	Memristor-less or Memristor based design	No. and Type of Active element (s)	No. of Passive Elements used	Grounded Passive Elements	Tunable	Requirement of Mutator/ Multiplier	Maximum Frequency	Experimental results
[10]	Memrister-less (Grounded Type)	3-CCII, 1-Multiplier	2-C, 3-R	Yes	No	Yes	5 kHz	Yes
	Memrister-less (Floating Type)	5-CCII, 1-OP-AMP, 1-Multiplier	2-C, 5-R	No	No	Yes	5 kHz	Yes
[11]	Memristor based (Microcontroller based)	1-OTA, 1-ADC, 1- Microcontroller	1-C, 2-R	No	No	Yes	5 Hz	No
[12]	Memristor-less (LDR based)	5- OP-AMP, 1-LDR	2-C, 13-R	No	No	Yes	10 Hz	Yes
[13]	Memristor-less	2-MO-OTA 1-Multiplier	2-C, 2-R	No	Yes	Yes	10 Hz	No
[14]	Memristor based	2-CCII, 1-ADC, 1- Microcontroller	2-C, 2-R	No	No	Yes	1 Hz	No
[15]	Memristor based	2-OP-AMP, 4- AD-844, 1-Multiplier	2-C, 9-R	No	No	Yes	86.6 Hz	Yes
[16]	Memristor based	2-CCII, 3-OP-AMP, 1-Multiplier	2-C, 4-R	No	No	Yes	900 Hz	No
[17]	Memristor-less	4-CCII,1-OP-AMP, 1-Varactor Diode	2-C, 6-R	No	No	Yes	8 kHz	No
[18]	Memristor-less	2-OP-AMP, 1-Multiplier, 1-Diode	2-C, 1-R	No	No	Yes	25 Hz	Yes
[19]	Memristor-less	2-CCII, 1-Multiplier	3-C, 1-R	No	No	Yes	2 kHz	Yes
[20]	Memristor based	2-VDTA(four OTA)	2-C	No	Yes	No	500 Hz	Yes
[21]	Memristor based	2DVCC (2-OTA, 2-CCII)	2-C, 2-R	No	Yes	No	100 Hz	Yes
[22]	Memristor-less	2 CCCII, 1CCII and 2 buffers	No (use of Parasitc capacitors)	--	Yes	No	80 MHz	No
[23]	Memristor based	2 CBTA, 1 Multiplier	2-C, 2-R	No	Yes	Yes	200 kHz	No
[24]	Memristor-less	4-OP-AMP, 1-CCCS 1-Multiplier	3-C, 2-R	Yes	Yes	Yes	10 Hz	No
[25]	Memristor-less	1-DXCCDITA 1-CMOS	2-C, 1-R	Yes	No	No	1 MHz	No

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