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Influence of element's parameters on the output characteristics of the voltage multiplier when powered from the inverter in resonance conditions

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Abstract: The article presents the influence of the parameters of the high voltage direct current (HVDC) generator with a multiplier, such as: leakage inductance of the high voltage (HV) transformer, capacitance, and the number of multiplier stages on the value of the output voltage, voltage ripple, power and frequency of the supply voltage as a function of the output current. The presented characteristics were obtained under the synchronization conditions of the inverter output voltage and current that powers the multiplier. The presented results will be useful when designing HVDC generators with Cockcroft-Walton multipliers.

Key words: high DC voltage generator, output characteristics, resonant inverter, voltage multiplier

1. Introduction

Voltage multipliers have many applications [1]. They are used to generate high DC voltage. They were very popular in CRT TVs and oscilloscopes. Currently, they can be found in, e.g. electrostatic spraying systems (powder coating, spraying of plant protection products), electrostatic segregation of materials [2], X-ray tube power supplies [3], systems for obtaining electricity from the electromagnetic field that surrounds us [4–6]. These are usually low power devices. In the case of designing multipliers with higher power (of the order of hundreds W and kW), it is necessary to analyze the impact of the power supply conditions and the parameters of the used elements on multiplier output characteristics. In the case of powering the multiplier from the inverter, through

the HV transformer, resonance phenomena occur. These phenomena have been described, e.g. in works [7,8]. [8] shows that the most advantageous, due to the stiffness of the output characteristics, is switching the inverter's transistors in the moments when the current supplying the multiplier changes direction. The voltage and current supplying the multiplier are then synchronized.

This article presents the influence of the values of parameters such as: the leakage inductance of the HV transformer, capacitor capacitance and number of multiplier stages on the value of the multiplier output voltage, output voltage ripple, frequency of the supply voltage as a function of the output current. The synchronization of the output voltage and current of the inverter will be maintained – the Load-Adaptive Frequency Modulation (LA-FM) was applied.

The presented results will be useful in the design of voltage multiplier powered by an inverter via an HV transformer. The motivation to study the impact of the element's parameters on the characteristics of the multiplier was the earlier design and construction, of two multipliers with rated powers of 60 and 160 W and an output voltage of 40 kV [8], used in sputtering and electrostatic separation devices [2]. The results presented in this article were obtained by means of a computer simulation (in LTSpice).

2. Phenomena occurring in the voltage multiplier when the supply voltage and current are synchronized

Figure 1 shows the structures of a multiplier with a multiplication factor n equal to 2, 4 and 8.

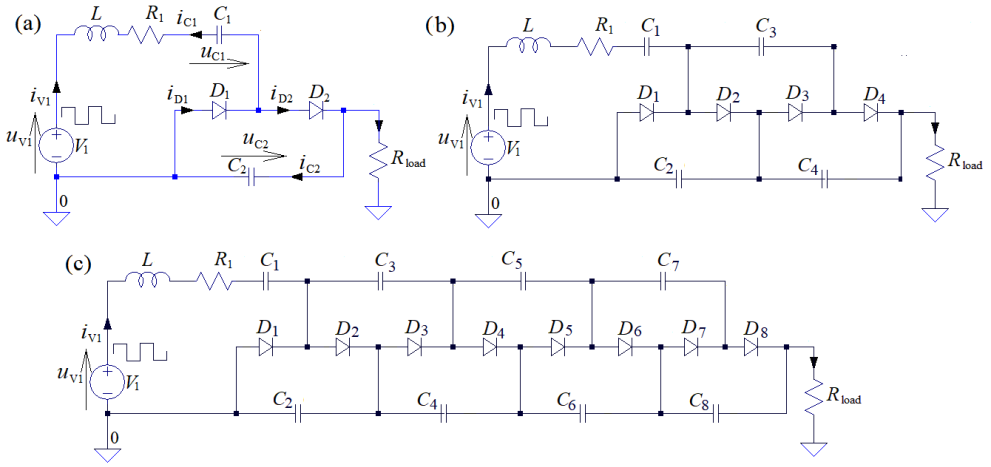

Fig. 1. A simplified scheme of voltage multiplier supplied by an inverter with an HV transformer (referred to the secondary side of the transformer): voltage doubler, $n = 2$ (a); voltage multiplier, $n = 4$ (b); voltage multiplier, $n = 8$ (c)

Figure 2 shows the waveforms of currents and voltages in these systems when supplied from a voltage inverter through a high-voltage transformer: input current and voltage of the voltage multiplier (i_{V1}, u_{V1}), multiplier output voltage and current (u_{Rload}, i_{Rload}), capacitor currents

($i_{C1}, \ldots, i_{C8}$) and diode currents ($i_{D1}, \ldots, i_{D8}$). It was assumed that the transistors are switched at the moments when the output current of the inverter is equal to zero (or close to them). This guarantees switching at zero current (ZCS) or switching at zero voltage (ZVS) and at the same time almost ZCS, which in real systems results in a practical reduction of commutation losses.

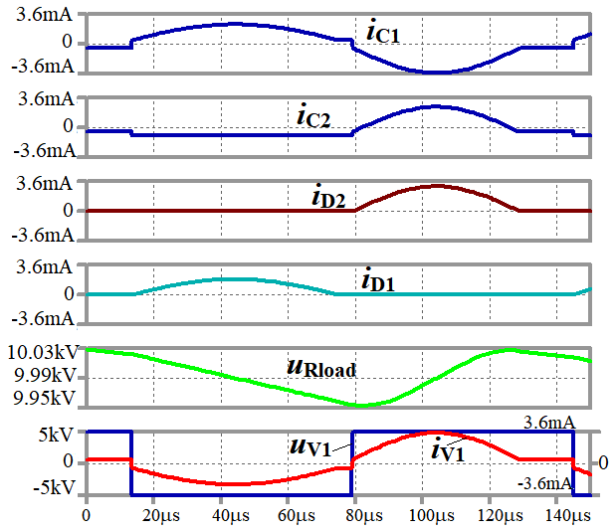

Fig. 2. Waveforms of currents and voltages in the voltage doubler system supplied by an inverter with an HV transformer (referred to the secondary side of the transformer): $n = 2$, $C = 1$ nF, $L = 0.5$ H, $R_{load} = 20$ MΩ, $f_s = 7.6$ kHz, $P = 5$ W

For the simplest voltage doubler (Figs. 1(a), 2), it is impossible to synchronize the switching with positive and negative half-waves of the current at the same time (when the supply voltage is in the form of half-period positive and half-period negative rectangular pulses). This is due to different durations of the current half-waves. The duration of the negative half-wave of the current is about 40% longer than the duration of the positive half-wave.

This is because during the negative half-wave the resonant circuit consists of the leakage inductance of the transformer and one capacitor. However, in the positive half-wave the leakage inductance and two capacitors are connected in series. With higher multiplication factor values, these differences decrease (Figs. 3, 4) and, for example, for $n = 8$ (Fig. 4) they are practically negligible.

In this article, we will deal with cases where $n > 2$ and $f_s \approx f_{fo}$, where f_s is the switching frequency of the transistors and f_{fo} is the free oscillation (natural) frequency. The maximum output power is obtained when the inverter is operating at the natural frequency of the system [8]. These cases ensure the minimization of transistor currents at the assumed output power. It is optimal from the point of view of power losses during conduction and switching. The natural frequency of the system depends on the capacity of the multiplier capacitors, the transformer's leakage inductances, multiplication factor and it is a function of the load. Load-Adaptive Frequency Modulation is required to ensure the synchronization. Power regulation is possible by changing the inverter supply voltage (amplitude modulation, AM) or pulse density modulation (PDM).

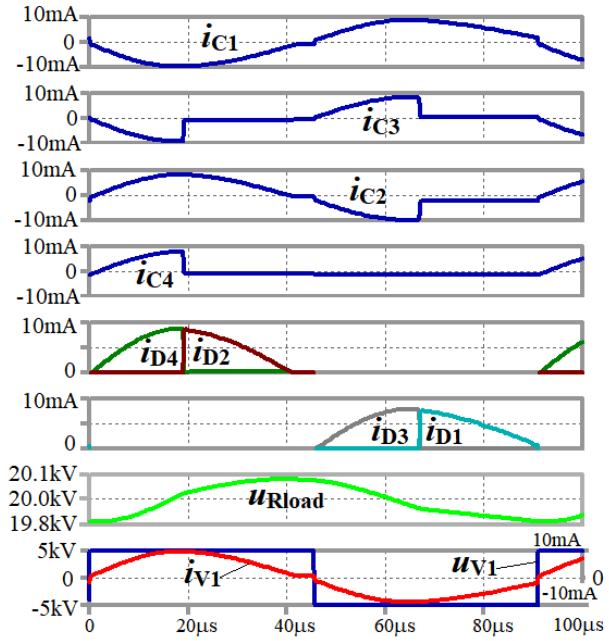

Fig. 3. Waveforms of currents and voltages in the voltage multiplier system supplied by an inverter with an HV transformer (referred to the secondary side of the transformer): $n = 4$, $C = 1$ nF, $L = 0.5$ H, $R_{\text{load}} = 20$ MΩ, $f_{\text{s}} = 11$ kHz, $P = 20$ W

During one period of the inverter operation for the multiplier from Fig. 1(a) (voltage doubler, $n = 2$), 2-time intervals can be distinguished (Fig. 2). In these intervals the equivalent resonant capacity C_{R} connected in series with the transformer leakage inductances are: $C_{\text{R}} = C/2$ (for the positive half-wave of current) and $C_{\text{R}} = C/1$ (for the negative current half-wave).

During one period of the inverter operation for the multiplier from Fig. 1(b) (multiplication factor $n = 4$), 4-time intervals can be distinguished (Fig. 3). In these intervals the equivalent resonant capacity C_{R} connected in series with the transformer leakage inductances are: $C_{\text{R}} = C/4$, $C/2$ (for the positive half-wave of current) and $C_{\text{R}} = C/3$, $C/1$ (for the negative half-wave of current).

Similarly, for a multiplier consisting of 8 capacitors and 8 diodes (Fig. 1(c)), there were 8-time intervals in which the equivalent capacities were [8]: $C_{\text{R}} = C/8$, $C/6$, $C/4$, $C/2$ for the positive half-wave of current and $C_{\text{R}} = C/7$, $C/5$, $C/3$, $C/1$ for the negative half-wave of current.

During the work cycle, the transformer's leakage inductances are connected in series with capacitors ranging from 1 to n. Therefore, the free oscillation frequency of the system is described by inequality (1) [8]:

$$\frac{1}{2\pi\sqrt{LC}} < f_{\text{fo}} < \frac{1}{2\pi\sqrt{LC/n}}. \tag{1}$$

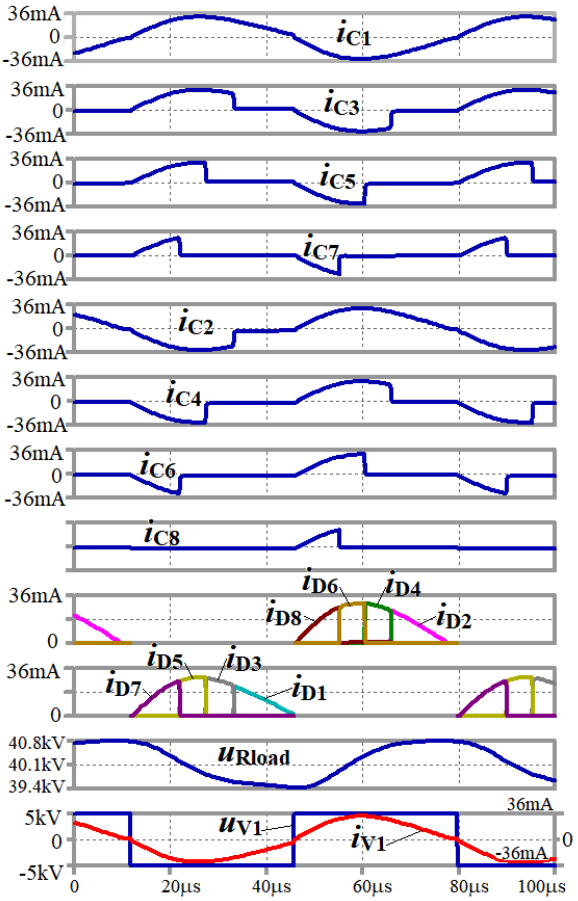

Fig. 4. Waveforms of currents and voltages in the voltage multiplier system supplied by an inverter with an HV transformer (referred to the secondary side of the transformer): $n = 8$, $C = 1$ nF, $L = 0.5$ H, $R_{\text{load}} = 20$ MΩ, $f_{\text{s}} = 14.7$ kHz, $P = 80$ W

When operating without load, the output voltage of the multiplier is given in Eq. (2):

$$U_{\text{Rload}}(I = 0) = |U_{\text{inv}}| \cdot \vartheta \cdot n = |U_{\text{V1}}| \cdot n, \tag{2}$$

where: $U_{\text{inv}} = \pm U_{\text{d}}/2$ for the half-bridge inverter or $U_{\text{inv}} = \pm U_{\text{d}}$ for the full bridge inverter, U_{d} is the inverter input voltage, U_{V1} is the inverter voltage seen at the transformer secondary side, ϑ is the transformer ratio.

Assuming no active losses and approximate sinusoidal shape of the supplying current (Fig. 4), the RMS value of inverter current (in the primary side of the transformer) is given in Eq. (3):

$$I_{\text{inv\_rms}} \approx \left(\sqrt{2}\pi/4\right) \cdot \vartheta \cdot n \cdot I_{\text{Rload}}. \tag{3}$$

The free oscillation frequency and output voltage as a function of the load will be determined by simulation and presented in the next chapter.

3. Characteristics of the voltage multiplier

Figure 5 shows the values of voltages, free oscillation frequency and equivalent capacitance of the whole system presented in Fig. 1(c), as a function of the output current of the multiplier. The simulation has been performed for the following data: $n = 8$, $C = 1$ nF, $L = 0.5$ H.

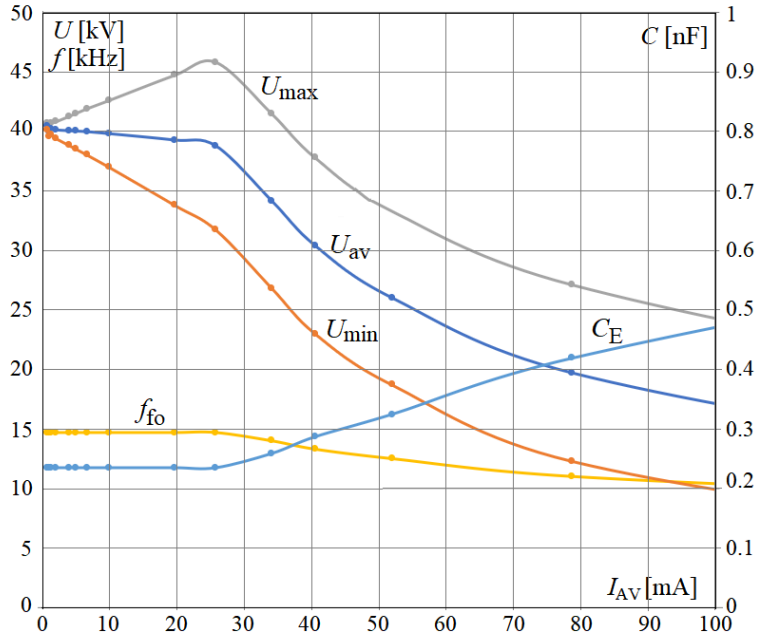

Fig. 5. Values of voltages, free oscillation frequency and equivalent capacitance of the system as a function of the output current of the multiplier; $n = 8$, $C = 1$ nF, $L = 0.5$ H

U_{max} and U_{min} are the instantaneous maximum and minimum values of the output voltage for a given load current (Fig. 4). U_{AV} is the average value of the output voltage. f_{fo} is the free oscillations frequency and C_E is the equivalent resonant capacitance of the system resulting from f_{fo} and transformer leakage inductance. C_E is described by Eq. (4):

$$C_E = \frac{1}{L(2\pi f_{fo})^2}. \tag{4}$$

The characteristics of the multiplier average output voltage and the ripple of this voltage (peak – peak, $U_{p-p} = U_{max} - U_{min}$) as a function of the load current of the voltage multiplier are shown also in Figs. 6 and 7. These characteristics were obtained for the assumed capacitances and leakage inductances $C_1 = \ldots = C_8 = C = 0.1$; 0.25; 0.5; 1 nF, $L = 0.5$ H for Fig. 6 and $C_1 = \ldots = C_8 = C = 1$ nF, $L = 0.5$; 1; 2.5; 5 H for Fig. 7.

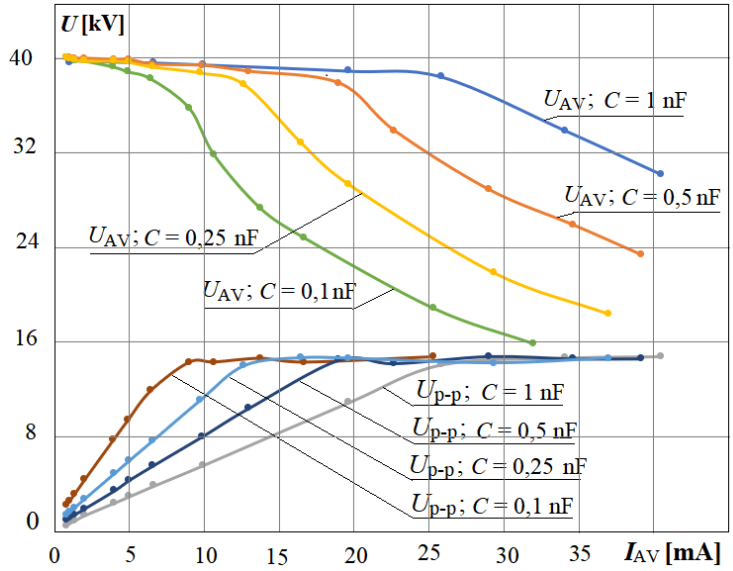

Fig. 6. Characteristics of average voltage U_{AV} and ripple voltage U_{p-p} as a function of average load current I_{AV} for C = 0.1; 0.25; 0.5; 1 nF, L = 0.5 H

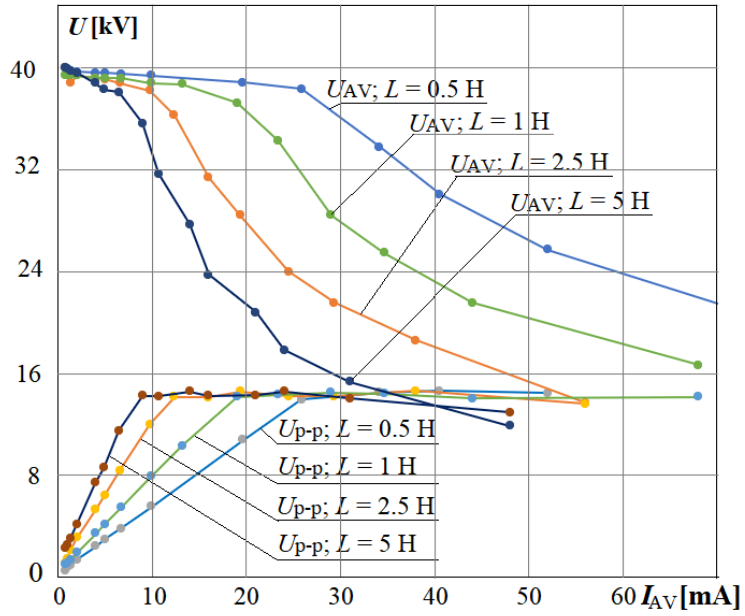

Fig. 7. Characteristics of average voltage U_{AV} and ripple voltage U_{p-p} as a function of average load current I_{AV} for C = 1 nF, L = 0.5; 1; 2.5; 5 H

In order to generalize the description of the phenomena occurring in the system, reference values were introduced and characteristics in relative values were presented. As reference values were adopted according to Eq. (5):

$$\begin{aligned} U_{\text{ref}} &= U_{\text{Rload}}\,(I_{\text{AV}} = 0) = |U_{\text{V1}}| \cdot n, \\ Z_{\text{ref}} &= n^2\sqrt{L/C}, \\ C_{\text{ref}} &= C, \\ f_{\text{ref}} &= f_{\text{fo}}\,(I_{\text{AV}} = 0), \\ I_{\text{ref}} &= \frac{U_{\text{ref}}}{Z_{\text{ref}}}, \\ P_{\text{ref}} &= U_{\text{ref}} \cdot I_{\text{ref}}. \end{aligned} \tag{5}$$

For such reference values, dimensionless values of voltage, currents and power are expressed using Eq. (6):

$$U^*_{\text{AV}} = \frac{U_{\text{AV}}}{U_{\text{ref}}}, \quad C^*_{\text{E}} = \frac{C_{\text{E}}}{C_{\text{ref}}}, \quad f^* = \frac{f_{\text{fo}}}{f_{\text{ref}}}, \quad I^*_{\text{AV}} = \frac{I_{\text{AV}}}{I_{\text{ref}}}, \quad P^* = \frac{P}{P_{\text{ref}}}. \tag{6}$$

The characteristics of the dimensionless: multiplier average output voltage U^*_{AV}, the ripple of this voltage (peak – peak, $U^*_{\text{p–p}} = U^*_{\text{max}} - U^*_{\text{min}}$), the power P^*, the frequency f^* of the inverter voltage during synchronization and the equivalent capacity C^*_{E} of the whole system as a function of the dimensionless load current are shown in Figs. 8 and 9. These characteristics were obtained (as before) for the assumed capacitances and inductances:

1) $C_1 = \ldots = C_8 = C = 0.1; 0.25; 0.5; 1$ nF, $L = 0.5$ H and

2) $C_1 = \ldots = C_8 = C = 1$ nF, $L = 0.5; 1; 2.5, 5$ H.

Figures 8 and 9 show two regions of the system operation, for the relative load current smaller than 1 and greater than 1, respectively. These regions are characterized by different behaviors in the variations of multiplier output voltage, power and voltage ripple, oscillation frequency and the equivalent capacity. In the second region, for a relative current greater than 1, the discharge of even-numbered capacitors with the load current is so intense that the voltages of these capacitors decrease. If the voltage of one of these capacitors becomes negative, the diodes connected in parallel to this capacitor switch to conduction. This capacitor is short-circuited by these diodes and the voltage across it is close to zero. For example, the capacitor C_8 is then short-circuited by two simultaneously conducting diodes D_7 and D_8. Short-circuiting a given capacitor through diodes eliminates this capacitor from the resonant circuit, changing both the structure of the circuit and the frequency of natural oscillations. Eliminating the capacitor reduces the number of time intervals in the oscillation period. In this case, for a relative current greater than 1, the current and voltage waveforms in the system are different than those shown in Figs. 2–4. In the event of a short circuit at the multiplier output, only the capacitor C_1 is a capacitive element of the resonant circuit.

During the simulation, it was assumed that: rectifier diodes are ideal, the transformer winding resistance was omitted, a 20 MΩ resistor was connected in parallel to each diode, which in the real systems symmetrized the voltages on each of the capacitors, causing the multiplier to be initially loaded with a resistance of 160 MΩ. The default values of the simulation control parameters were adopted as in the *Control panel/Spice* program window. Additionally, a *Maximum Timestep* of 0.01 μs was assumed.

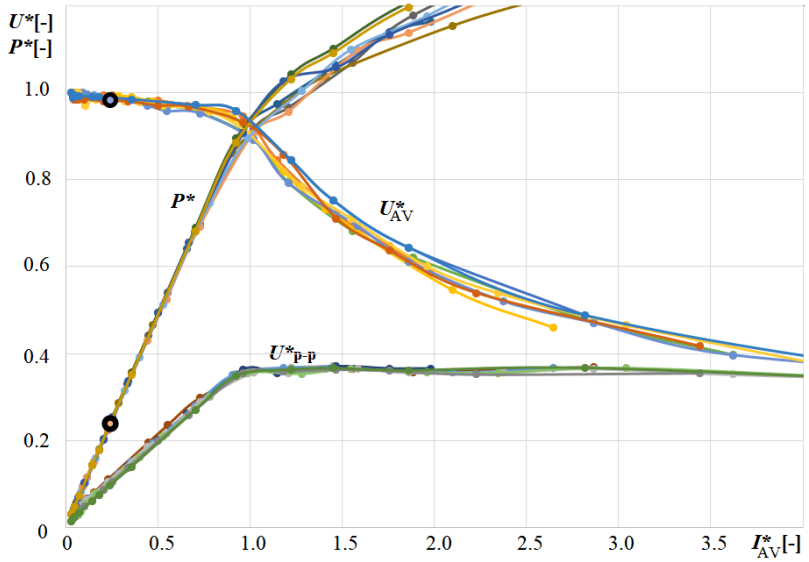

Fig. 8. Characteristics of the relative values of: multiplier average output voltage U^*_{AV}, the ripple of this voltage $U^*_{\mathrm{p-p}}$, the power P^* during synchronization inverter voltage and current as a function of the relative values of load current for: 1) $C = 0.1; 0.25; 0.5; 1$ nF, $L = 0.5$ H and 2) $C = 1$ nF, $L = 0.5; 1; 2.5; 5$ H; (these points marked with black circles are the result of an experimental test - see chapter 4)

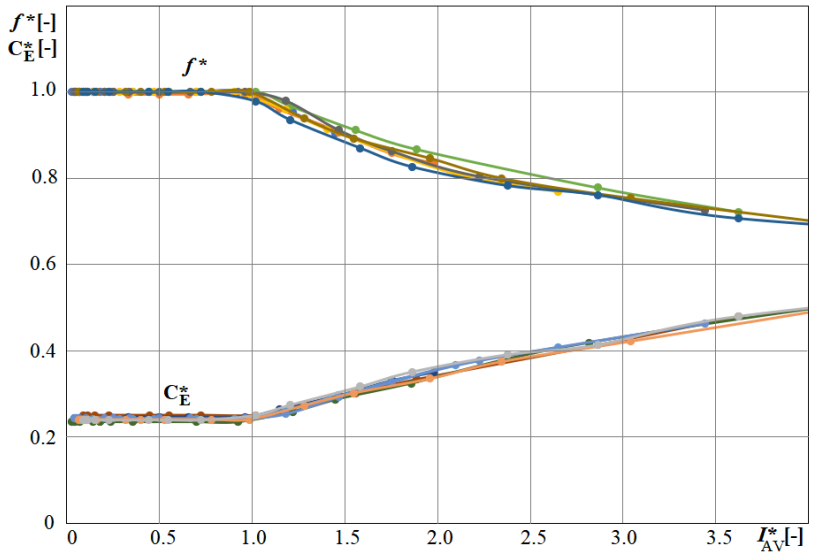

Fig. 9. Characteristics of the relative values of: the multiplier swiching frequency f^* and the equivalent capacity $C*_{\mathrm{E}}$ of the whole system during synchronization as a function of the relative values of load current for: 1) $C = 0.1; 0.25; 0.5; 1$ nF, $L = 0.5$ H and 2) $C = 1$ nF, $L = 0.5; 1; 2.5; 5$ H

4. Experimental setup used for electrostatic segregation

The prototype multiplier system with a multiplication factor $n = 8$ (without electrical insulating compound) is shown in Fig. 10(a). The printed circuit board (PCB) has been designed so that it is possible to make a multiplier with a maximum factor of $n = 10$. The circuit diagram including real components is in Fig. 10(b). DD1600 diodes with a maximum reverse voltage of 16 kV were used to build the multiplier. The CC10k-2N2 capacitors were used with a capacity of 2.2 nF and a maximum voltage of 10 kV. Each capacitor shown in the simplified diagram in Fig. 1 consists of two CC10k-2N2 capacitors connected in series, with a resultant capacity of 1.1 nF. In order to ensure an even division of the capacitor voltage, high-voltage 62 MΩ 1 W 10 kV resistors are connected in parallel to each capacitor. The multiplier output is additionally equipped with resistors that limit the current in the event of a short circuit at the output, e.g. when an arc discharge occurs. The voltage oversizing of the elements was intentional so that the system could operate in a wider voltage range in the future. Oversizing also ensured greater durability of the elements. The HV transformer was built using a UY16-5857 core made of PC40 ferrite. The turns ratio ϑ was approximately 31, which made it possible to obtain a voltage in the range of 0–5 kV on the secondary side when powered by a half-bridge inverter with an input voltage of approximately 0–320 V. The leakage inductance and winding resistance seen from the secondary side of the transformer were 1.105 H and 1354 Ω, respectively. The inductance measured from the secondary side (when the primary winding was open) was 11.67 H. Measurements were made with CHY41R and BM857 multimeters. The tests were initially carried out with reduced supply voltage and a multiplier without a silicone electrical insulating compound. This made it possible to measure voltages and currents while maintaining safety.

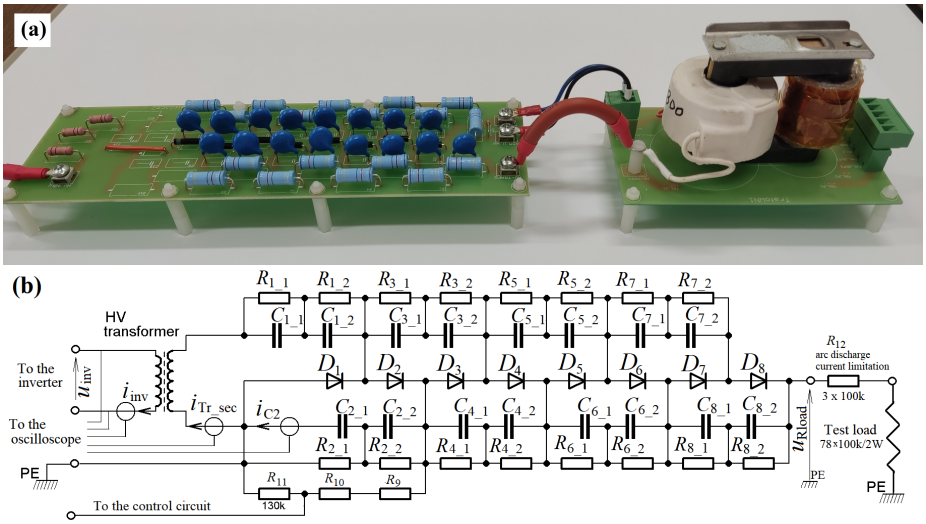

Fig. 10. View of the printed circuit board and high-voltage transformer (a) of the multiplier prototype with a factor of $n = 8$ and a schematic diagram (b) with marked places of connecting measuring devices; all resistors, unless otherwise noted, are 62 MΩ

The current was recorded using an oscilloscope (SDS1052DL) only in places where the voltage relative to the earth potential was not high (Fig. 10(b)). The inverter output voltage, applied to the primary winding of the HV transformer, was also recorded using an oscilloscope. For oscilloscope measurements, a Rogowski current probe (CWTUM/1/B) and a separation differential probe (TT-SI9001) were used. Measurements of the average value of the output voltage were made using the HV probe (HVP-40) and the BM257s multimeter. Example oscillograms showing current and voltage waveforms in the system during tests at reduced voltage are shown in Fig. 11. Figure 12 shows the simulation results of the system with the parameters of the elements used in the tests. It was assumed that $u_{\text{inv}} = u_{\text{V1}}/\vartheta$ and $i_{\text{inv}} = i_{\text{V1}} * \vartheta$, where u_{inv}, i_{inv} are the voltage and current of the inverter (Fig. 10(b)) and u_{V1}, i_{V1} are the voltage and current of the source in the equivalent diagram (as in Fig. 1). Figure 12(a) shows the results when using a simplified transformer model, taking into account only leakage inductance and winding resistance (as in Fig. 1). Figure 12(b) shows the results when also taking into account the main inductance (equivalent transformer diagram of a T-type) and the winding capacitance (approx. 18 pF) viewed from the secondary side. In both cases, the shapes of the current and voltage waveforms obtained by simulation were similar to the waveforms from the oscillograms. This was the basis for assuming that the characteristics obtained by simulation were close to the real ones. Taking into account the magnetization inductance and winding capacitance (Fig. 12(b)) obviously gave more accurate waveforms. When simulating the system with elements as in Fig. 10(b), the characteristics of the diodes were approximated by semi-straight lines where the threshold voltage $U_{\text{F}} = 5$ V and the dynamic resistance $r_{\text{F}} = 10\ \Omega$. Other control parameters of the simulation were default when *Maximum Timestep* was 0.01 μs.

Reference values calculated according to Eq. (5) for the test system and the transformer primary side voltage of 32.8 V were:

$U_{\text{ref}} = 32.8 \cdot 31 \cdot 8 \approx 8.13$ kV,

$Z_{\text{ref}} = (8)^2 \cdot (1.105/1.1e - 9)^{1/2} \approx 2.03$ MΩ,

$f_{\text{ref}} \approx 9.8$ kHz,

$I_{\text{ref}} = U_{\text{ref}}/Z_{\text{ref}} \approx 4.01$ mA,

$P_{\text{ref}} \approx 33$ W.

The measured multiplier output voltage was 7.98 kV. The relative values of voltage, current and power at the multiplier output were:

$U^*_{\text{AV}} \approx 7.98\ \text{kV}/8.13\ \text{kV} \approx 0.982$,

$I^*_{\text{AV}} = (7.98\ \text{kV}/8.1\ \text{MΩ})/4.01\ \text{mA} \approx 0.246$,

$P^* \approx 7.86/33 \approx 0.238$.

The experimentally determined relative values of voltage and power lie on the characteristics determined by simulation (Fig. 8, points marked with a black circles).

For industrial use, to operate at full voltage, the multiplier had to be placed in an electrical insulating compound. The devices for electrostatic sputtering (40 kV, 60 W) and electrostatic segregation [2, 8] of plastics or plastics and metal chips (40 kV, 160 W) were designed and tested. This system was made for the Institute of Polymer Materials and Dyes Engineering (IMPIB) in Toruń. Operational tests confirmed its correct operation. As a result of the tests, it was confirmed that the highest rigidity of the external (current-voltage) characteristic is obtained if the inverter transistors are switched synchronously with the wave of the current supplying the multiplier. It was also noticed that above a certain value of the output current of the multiplier, the external characteristic decreases much faster. All these observations confirmed the results of the simulation studies presented in this article.

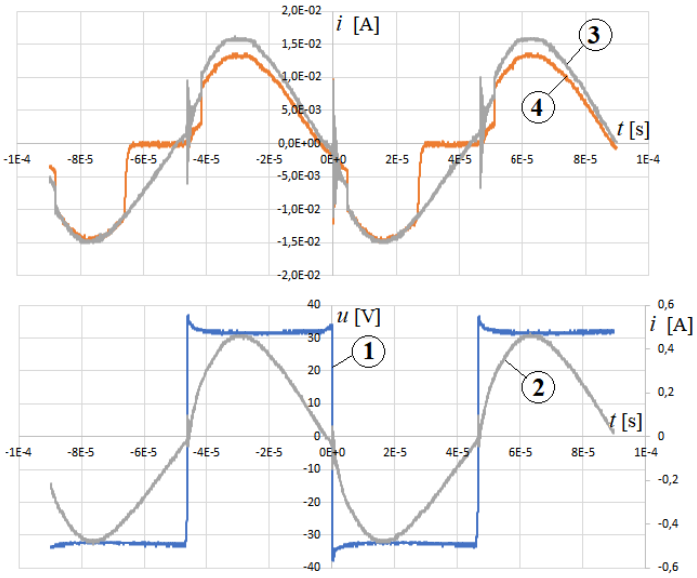

Fig. 11. Current and voltage waveforms in the system during tests at reduced voltage: 1 – u_{inv}, 2 – i_{inv}, 3 – $i_{\mathrm{Tr\,sec}}$, 4 – i_{C2}

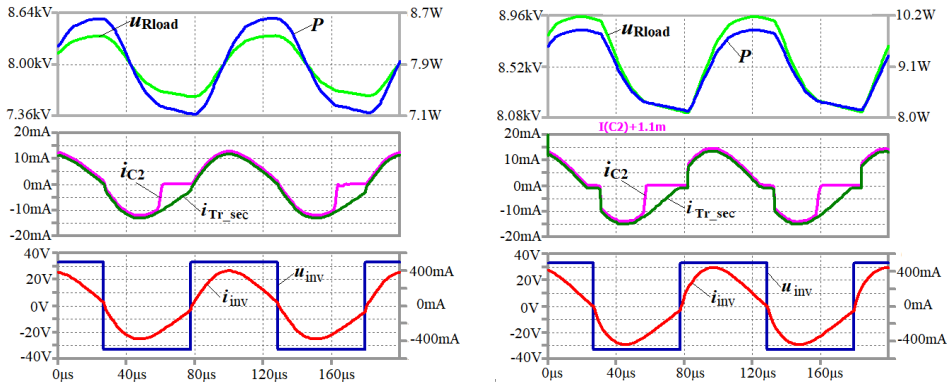

Fig. 12. Current and voltage waveforms in the system obtained by simulation for data as in the test: (a) for a simplified transformer model; (b) T-type transformer model with additional winding capacity taken into account

The block diagram of the power supply and control system of the industrially applied voltage multiplier is shown in Fig. 13. This figure also shows the idea of electrostatic segregation of various plastics or metal and plastics chips. Figure 14 shows a photo of the converter whose block diagram is shown in Fig. 13. The view of the voltage multiplier (in an electrical insulating compound) of the 160 W 40 kV system used to electrostatic segregation is presented in Fig. 15.

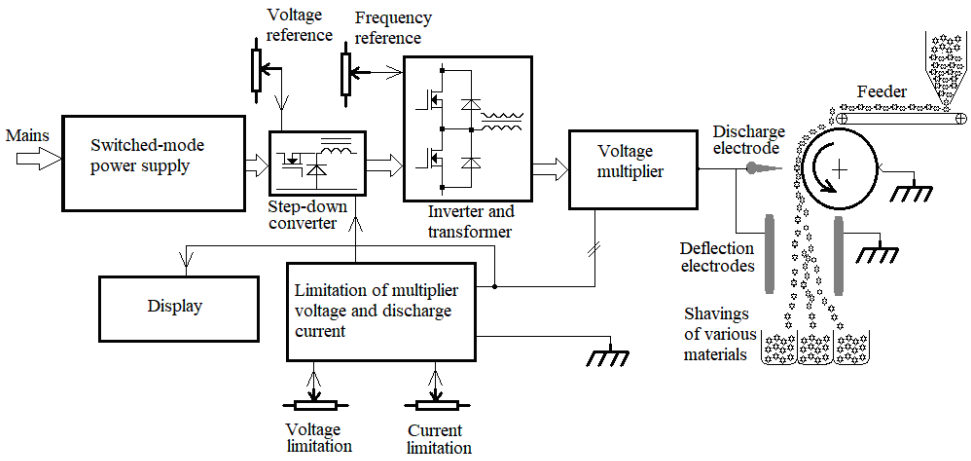

Fig. 13. The block diagram of the power supply and control system of the tested voltage multiplier used for electrostatic segregation of various plastics and matal chips

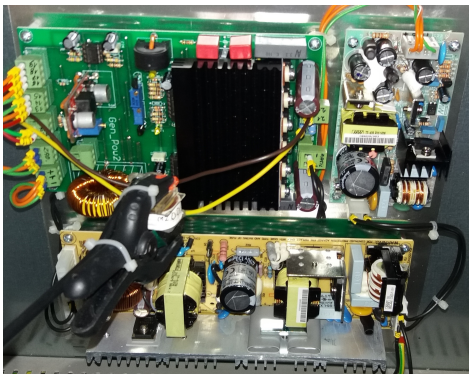

Fig. 14. The view of the inverter of the 160 W 40 kV used for electrostatic segregation [8]

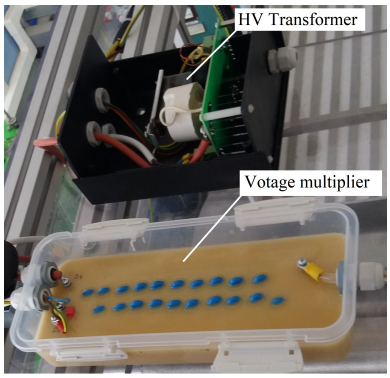

Fig. 15. The view of the voltage multiplier and HV transformer of the 160 W 4 kV system used for electrostatic segregation [8]

5. Conclusions

The presented simulation studies show that for the assumed inductance values $L = 0.5; 1; 2.5; 5$ H and constant capacitance $C = 1$ nF, practically the same characteristics were obtained in relative values. Similar simulation studies were carried out for a constant value of inductance $L = 0.5$ H and capacitance $C = 0.1; 0.25; 0.5; 1$ nF. Regardless of changes of L or C, the characteristics of the system in relative values are the same.

1. Appropriately selected reference values allow one to present the characteristics of the multiplier in relative values, regardless of the parameters of its components.

2. For a relative load current less than 1, the following can be observed:
   - the $U^*_{AV} = f(I^*_{AV})$ characteristic of the multiplier output voltage decreases slightly for the inverter operation frequency equal to free (natural) oscillation frequency of the multiplier system (at Load-Adaptive Frequency Modulation),
   - the power P^* and voltage ripple U^*_{p-p} are proportional to the load current I^*_{AV}, if $I^*_{AV} = 1$ then P^* is close to 1,
   - the free oscillation frequency $f^* = \text{const} = 1$ and the equivalent capacity $C^*_E = \text{const}$.
3. For a relative load current greater than 1, the following can be observed:
   - the $U^*_{AV} = f(I^*_{AV})$ characteristic of the multiplier output voltage decreases quite quickly,
   - the power P^* grows slower and the voltage ripple U^*_{p-p} is constant,
   - the free oscillation frequency of the system decreases and the equivalent capacity increases, in the event of a short circuit on the output, the equivalent capacitance C^*_E is close to 1.
4. The conducted research will greatly facilitate the process of designing voltage multipliers in which the inverter output voltage and current are synchronized and resonance phenomena are used. In the initial design phase, the relative output current should be determined. Then, based on the characteristics from Figs. 8 and 9, it will be possible to determine without additional simulations and calculations whether the external characteristics will be stiff, whether the frequency of natural oscillations will be constant and what will be the ripples. If the relative load current in the entire operating range is less than 1, then the frequency of natural oscillations will be practically constant. It will then be possible to use constant frequency switching of transistors instead of Load-Adaptive Frequency Modulation. This will simplify the design of the inverter.

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