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Dual Second Order Generalized Integrator – Phase Locked Loop technique applied to a distorted grid-connected solar energy based on a Z-Source Inverter

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Abstract: In this paper, a Dual Second Order Generalized Integrator_Phase Locked Loop (DSOGI_PLL) technique applied to the Photovoltaic (PV) system supplying a Z-Source five-level Inverter (ZSI) is presented. The ZSI assures the increasing voltage of the PV system and provides the desired output DC at the input of the five-level Neutral Point Clamped Inverter (5L_NPCI), without any control which reduces the complexity of the overall system, this is due to the impedance network in its structure. We use Z-Source in order to eliminate the controlled DC bus as well as the use of the DC-DC Boost converter as an intermediary. A DSOGI technique is employed to control and optimize the energy quality, especially in distorted grid conditions and allows one to obtain a very low value of Total Harmonic Distortion (THD) which means lower peak currents, and higher efficiency. Low THD is an essential feature in power systems that international standards such as IEC 61000-3-2, and IEEE-519 set limits on the harmonic currents of various classes of power equipment connected to a distorted three-phase grid. Compared to the classic structure of inverters, the NPC five-level inverter presents a very high performance.

Key words: DSOGI_PLL, distorted grid-connected PV system, NPC five-level Inverter, THD, Z-Source

Essential abbreviations

DSOGI_PLL	Dual Second Order Generalized Integrator_Phase Locked Loop
SRF-PLL	Synchronous Reference Frame-Phase Locked Loop
CDSC_PLL	Cascaded Delayed Signal Cancellation_Phase Locked Loop
MDSC_PLL	Multiple Delayed Signal Cancellation_Phase Locked Loop
ZSI	Z-Source Inverter
5L_NPCI	Five-level Neutral Point Clamped Inverter
THD	Total Harmonic Distortion
THD(i)	Total Harmonic Distortion of current
THD(v)	Total Harmonic Distortion of voltage
PD-SPWM	Phase Disposition-Sinusoidal Pulse Width Modulation
PS-SPWM	Phase Shifted-Sinusoidal-Pulse Width Modulation
LS-SPWM	Level Shifted-Sinusoidal-Pulse Width Modulation
APOD-SPWM	Alternating Phase Opposition Disposition-Pulse Width Modulation
POD-SPWM	Phase Offset Disposition-Pulse Width Modulation
MLI	Multilevel Inverter
LPF	Low-Pass-Filter
BPF	Band-Pass-Filter
QSG	Quadrature-Signal-Generator
PSC	Positive-Sequence-Calculator

1. Introduction

Renewable energy sources, particularly solar, are gaining recognition and adoption in the energy sector, and they are considered one of the cleanest and most convenient energy sources for future energy demand [1, 2]. The photovoltaic system has the advantages of safety, reliability, no exhaustion risk, and a short construction period, which is in line with future development needs and is most suitable for any location, as solar irradiation is available throughout the year [3, 4]. Grid-connected PV systems have lately gained popularity since they do not require physical storage devices (batteries), lowering the investment cost in grid-connected photovoltaic systems [5].

In [26], a DC/DC boost converter is used to increase and control the voltage at the output of the PV system, and in this paper, the DC/DC converter is replaced by the ZSI network, which provides very high performance without any control (boost).

The ZSI has received attention for its features of an inherent buck-boost capability in a single conversion stage, improved output voltage gain, increased reliability in [6,22], and provides desired output AC voltage [7], so this circuit may be looked at as a buck-boost converter that precisely meets the requirements of grid-connected systems [8]. The type of DC/AC converter used is the 5L_NPC three-phase inverter. It consists of three legs and four DC voltage sources. Each leg has eight switches (3X8) which are managed using the Phase Disposition-Sinusoidal Pulse Width Modulation (DP-SPWM), approach and six diodes (06 diodes per leg), each two of the six clamp diodes are linked to the DC link's neutral point. Compared to a three-level inverter, the output waveform's THD of a multilevel inverter (MLI) is reduced when the number of levels increases [9]. Also, as shown in [24], the increase in current reference causes decreases in THD, Table 1 shows the comparison between the THD in [24,27] and our numerical simulation results of the THD. A coupling inductor between the 5L_NPC inverter and the distorted grid is necessary for filtering the inverter's output current, and it is a key method for ripple reduction and fast transient in pulse width-modulated power converters [23], its value (L_i) is related to the quality of the current.

Classic PLL methods cannot ensure the connection and synchronization with distorted and unbalanced networks, such as the Synchronous Reference Frame Locked Loop (SRF-PLL), because it will not perform in the desired way. Grid angle tracking is not achieved in real time which leads to the undesirable operation of power electronic loads [19,25]. For this reason, it is imperative to use the DSOGI_PLL method with Low-Pass-Filter (LPF), the main objective is the calculation of a stable and undisturbed phase angle grid during any voltage conditions. Our control is based on two steps, the first one is based on the mentioned application (DSOGI_PLL) aiming to improve the frequency and maintain its value (50 Hz) in the case of a distorted grid. The second step is the modeling approach and mathematical decoupling in the Direct-Quadrature (DQ) transformation reference frame by using the inverse park transformation (d, q to abc). V_{abc} voltages ($V_{a\text{ref}}$, $V_{b\text{ref}}$ and $V_{c\text{ref}}$) are used as references in the PD-PWM controller of the 5L_NPC inverter. In the proposed system our contribution focuses on the DSOGI_PLL, ZSI and 5L_NPC inverter to ensure a low harmonic distortion. In the literature, the THD is in the order of 2 to 4%, as presented in Table 1.

Table 1. Comparison of numerical simulation results of the THD

Inverter	**Reference current (A) or power (kW)**	**THD%**
In [24]	(6, 10) A	(4.2, 2.9)
Three level NPC in [27]	(50.52, 40.3) (kW)	(2.42, 3.32)

2. System configuration and operating principle

The proposed system's schematic, presented in Fig. 1, is composed of four PV arrays, two Z-Sources networks, a 5L_NPC inverter, a coupling inductor, a current controller, the PD-SPWM strategy (modulation control), and the DSOGI control method applied to the distorted three-phase grid.

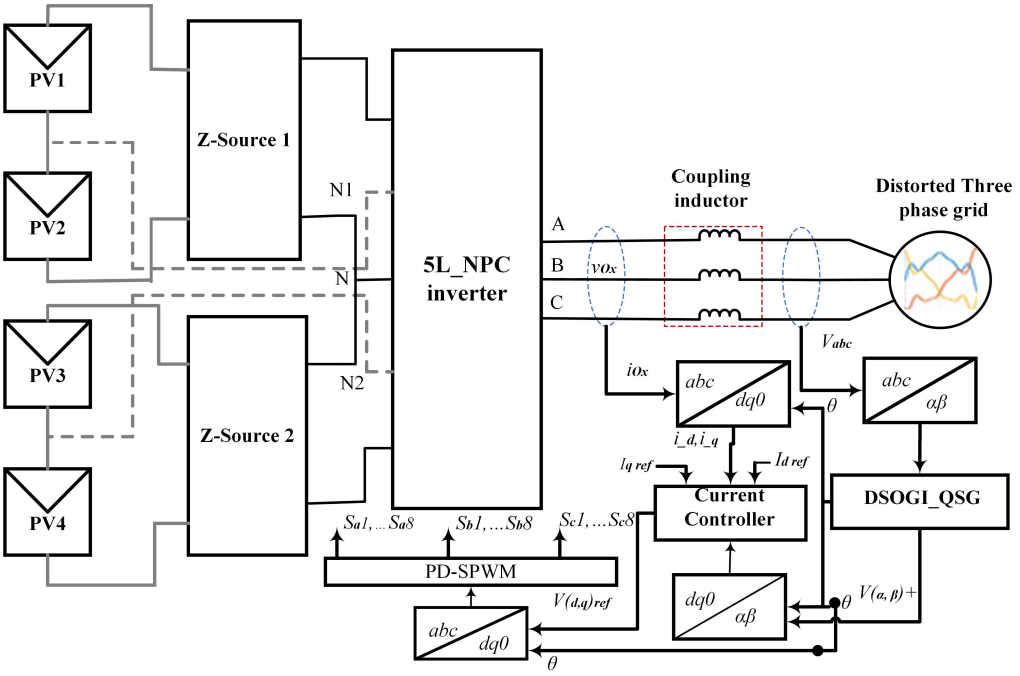

Fig. 1. General schematic andTopology of five-level Z-Source diode-clamped_inverter connected to the distorted three-phase grid

2.1. Solar array

A photovoltaic system's basic unit is the solar cell; a PV panel or PV module is formed by connecting solar cells in series. PV arrays are formed when these modules are joined in series and parallel [10]. The single-diode circuit model is the most commonly used model in solar cell modeling to estimate energy production [11]. All parameters of the model use the data displayed in Table 2. The current equation can be written as (1), where I is the solar cell current, I_{pv} is the photo-current, is directly proportional to solar irradiance (G), I_D is the diode current, and I_{sh} is the current flowing through the shunt resistor.

$$I = I_{pv} - I_D - I_{sh}, \tag{1}$$

$$I_{pv} = \frac{G}{G_n}(I_{pvn} + K_i \Delta T), \tag{2}$$

where: $\Delta T = T - T_n, T_n = 25°\text{C}$, G is the incident of irradiation on the module, and $G_n = 1000\,\text{W/m}^2$ at standard condition (STC), I_{pvn} is the photo-current at STC, and K_i is the thermal coefficient at short-circuit current (I_{sc}).

Table 2. Parameters of PV model

Description	**Rating**
Cells per module (Ncell)	60
N of PV array	4
Parallel strings (NP)	10
Series-connected modules per string (NS)	5
Maximum power P_{mppt} (W)	213.15
Voltage at maximum power V_{mp} (V)	29
Current at maximum power I_{mp} (A)	7.35
Open circuit voltage V_{oc} (V)	36.3
Short-circuit current I_{sc} (A)	7.84
Referenced solar irradiance G_n (W/m^2)	1000

2.2. Z-Source inverter topology and analysis

A configuration of two ZSI networks connected to the photovoltaic system and a three-phase grid (distorted grid) via the 5L_NPC inverter, as illustrated in Fig. 2. The ZSI has an exclusive equal impedance network using two inductors ($L1$, $L2$) and two capacitors ($C1$, $C2$) of equal value, which are connected in an X-shape with series inductors and diagonal capacitors [12]. This structure can be applied to all power converters [13]. In Fig. 2 the upper clamping leg is connected to the neutral point N1 between PV sources (PV1 and PV2), and the lower clamping leg is connected to another neutral point N2 formed between PV3 and PV4, respectively. Aside from these two links, the middle clamping leg is connected to the neutral point N, which is formed by cascading two ZSI. These ZS networks would increase DC voltage equally if the inverter operated properly; therefore, N is a real-neutral point in the inverter operation, which can be illustrated by the simplified equivalent circuits shown in Fig. 3, Fig. 4(a) and Fig. 4(b).

The ZSI has three operating modes that are determined by the switching of the 5L_NPC inverter, as given below:

– Non-shoot-through mode (active condition): in this case, the DC source is connected to two ZSIs (V_{dc}), each one contains two identical inductors and capacitors. The capacitors are charged, and the energy passes to the grid via inductors, as shown in Fig. 3.
– Upper shoot-through mode (UST): The upper short circuit is effectively inserted by turning ON switches S_x1, S_x2, S_x3, S_x4, and S_x5 with D_x4 and $D1$ conducting, D_x1 and $D2$ blocking and the lower Z-source network is staying in a non-shoot-through state, as shown in Fig. 4(a).
– Lower shoot-through (LST): The same analytical strategy when applied to the lower partial shoot-through state shown in Fig. 4(b) would similarly reveal that it is introduced by turning ON S_x4, S_x5, S_x6, S_x7, and S_x8 with D_x3 and $D4$ conducting, D_x5 and $D3$ blocking, and the upper Z-source remaining in its non-shoot-through state.

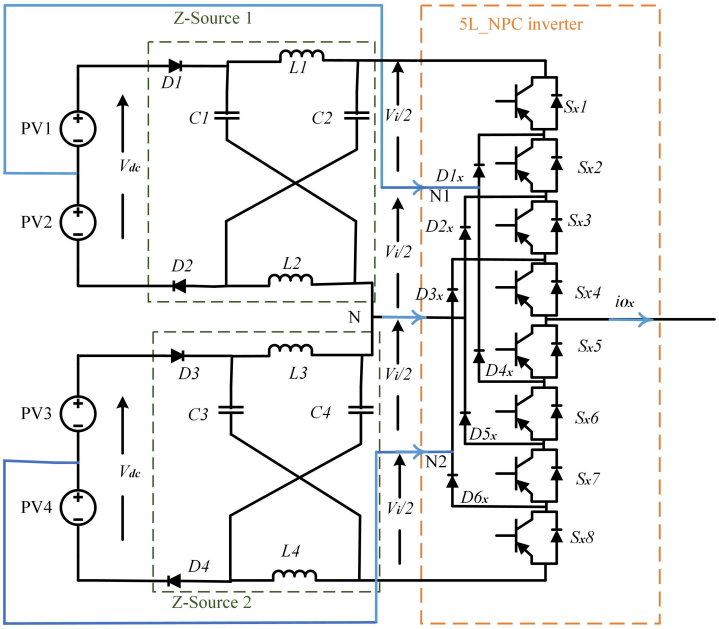

Fig. 2. Structure of Z-Source NPC five-level inverter

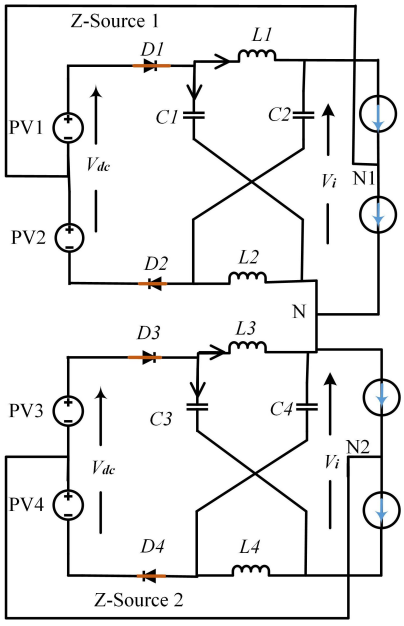

Fig. 3. Equivalent circuit of Z-SI in the non-shoot-through state

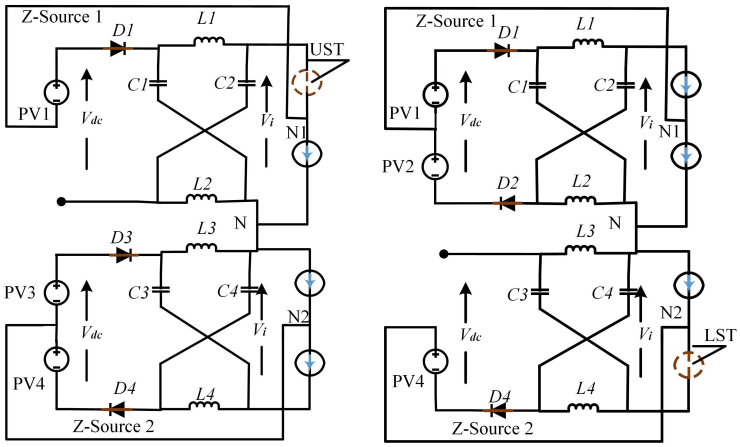

Fig. 4. Equivalent circuit of ZSI in upper shoot-through state (a); lower shoot-through state (b)

Table 3. Upper and lower shoot-through state of the 5L_ZSI

State name	**Conducting switch *X* (*a*, *b*, or *c*)**	**Diodes state**
Upper shoot-through	S_x1, S_x2, S_x3, S_x4, and S_x5	D_x4 and $D1$ conducting D_x1 and $D2$ blocking
Lower shoot-through	S_x4, S_x5, S_x6, S_x7, and S_x8	D_x3 and $D4$ conducting D_x5 and $D3$ blocking

Table 3 summarizes the upper and lower shoot-through state of the 5L_ZSI.

During (upper or lower) shoot-through intervals, the inductor voltage equation can be written as (3):

$$V_{L1} = V_{L2} = V_{dc}. \tag{3}$$

In the non-shoot-through mode, the inductor voltage (V_{L1}, V_{L2}), capacitor voltage (V_{c1}, V_{c2}), and ZS output voltage can be expressed using (4) and (5):

$$V_{L1} = V_{L2} = \frac{2T_0}{T-2T_0}V_{dc} \quad V_c = 2V_{dc} - V_{L1} = \frac{2T-2T_0}{T-2T_0}V_{dc}, \tag{4}$$

$$V_i = V_c - V_{dc} = \frac{2T}{T-2T_0}V_{dc}, \quad V_{dc} = 2V_{\mathrm{PV}}, \quad V_{\mathrm{Output\_ZS}} = V_i, \tag{5}$$

$$V_{\mathrm{Output\_ZS}} = \mathrm{B}V_{dc}, \quad \mathrm{B} = \frac{V_{\mathrm{Output\_ZS}}}{2V_{\mathrm{PV}}}, \tag{6}$$

where B is the boost factor and T_0 is the duration of the shoot-through during the switching period T ($2T_0 < T$). According to (4) and (5), the DC voltage of ZS alternates between $V^*_{dc}(2T/T - 2T_0)$ and $V^*_{dc}(T/T - T_0)$. The output voltage's AC peak value, $\hat{v}_{Ox}$, can be estimated via (7).

$$\hat{v}_{Ox} = M\frac{\hat{v}_t}{2} = MBV_{dc}, \tag{7}$$

where $\hat{v}_t$ is the peak value of the DC output voltage "V_t" and M is the modulation index.

2.3. Five-level NPC inverter and its control PD-SPWM

The architecture of the five-level NPC inverter VSI (shown in Fig. 2), which consists of three legs X (A, B, and C), where the nominal voltage of the two DC voltages of Z-sources is "V_t" (total voltage of the two ZSI; $V_t = V^*_{\text{Output\_ZS}}$), every leg has 8 bidirectional switches, 6 in series and 2 in parallel, and 2 diodes to get 0 voltage (neutral). Every switch is composed of a transistor and a diode in anti-parallel. Table 4 shows the switch state and its influence on the output voltage and current for phase "A" ($x = a$) [14].

Table 4. Switching state of 5L_NPC inverter (for phase A only)

Switch state								**Output voltage**
S_a1	S_a2	S_a3	S_a4	S_a5	S_a6	S_a7	S_a8	$V(x = a)$
1	1	1	1	0	0	0	0	V_i
0	1	1	1	1	0	0	0	$V_i/2$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_i$
0	0	0	0	1	1	1	1	$-V_i/2$

Table 4 presents the control of the switching sequences that makes the system fully controllable at five levels and makes it possible to get the following output voltages (V_i, $V_i/2$, 0, $-V_i/2$, V_i) using the PD-SPWM. The principle of this strategy is presented in section 2.4.

2.4. Phase Disposition – Sinusoidal Pulse Width Modulation (PD-SPWM) based on the *dq* control

The Sinusoidal Pulse Width Modulation (SPWM) control technique is the most popular among all and widely utilized in industrial applications. SPWM uses several triangular carrier waves, and for each phase, there is a signal reference. It is categorized into Phase Shifted (PS)-SPWM, and Level Shifted-Sinusoidal (LS)-SPWM. The PS-SPWM can be categorized into Alternating Phase Opposition Disposition (APOD)-SPWM, Phase Disposition (PD)-SPWM, and Phase Offset Disposition (POD)-SPWM [15]. This paper proposes the PD-SPWM strategy for the 5L_NPC inverter because it has the lowest THD compared to the other modulation strategies [16].

Figure 5 shows the arrangement of PD-SPWM for switching of five voltage levels of the 5L_NPC inverter. It is obvious that the modulation index is equal to 0.81 and the frequency of the carrier (f_c) is 1000 Hz ($f_c = 20 \times f$) in triangle form. Carrier 1 ($SC1$) is used to generate switching signals of $\{S_x1, S_x5\}$. Carrier 2 ($SC2$) is employed to generate switching signals for $\{S_x2, S_x6\}$. Carrier 3 ($SC3$) is used to generate switching signals for $\{S_x3, S_x7\}$, and carrier 4 ($SC4$) is performed to generate switching signals for $\{S_x8, S_x4\}$. As shown in the figure above, the four carriers ($SC1$, $SC2$, $SC3$, and $SC4$) are in phase.

The current loop regulators are developed based on the following: (8), (9), and (10). Figure 6 shows the DQ control loops for the proposed system, where (V_{d_g}, V_{q_g}) and (i_d, i_q) are the real and imaginary components of grid voltage (V_g) and inverter current (i_{Ox}), respectively, in the ($d - q$) frame as represented by (7) and (8).

$$V_g = V_{d\_g} + jV_{q\_g}, \tag{8}$$

$$i_{Ox} = i\_d + ji\_q, \tag{9}$$

$$L_i \frac{\mathrm{d}i_{Ox}}{\mathrm{d}t} = v_{Ox} - V_g, \tag{10}$$

$$V_d = L_i \frac{\mathrm{d}i\_d}{\mathrm{d}t} - wL_i i\_q + V_{d\_g}, \tag{11}$$

$$V_q = L_i \frac{\mathrm{d}i\_d}{\mathrm{d}t} + wL_i i\_d + V_{q\_g}. \tag{12}$$

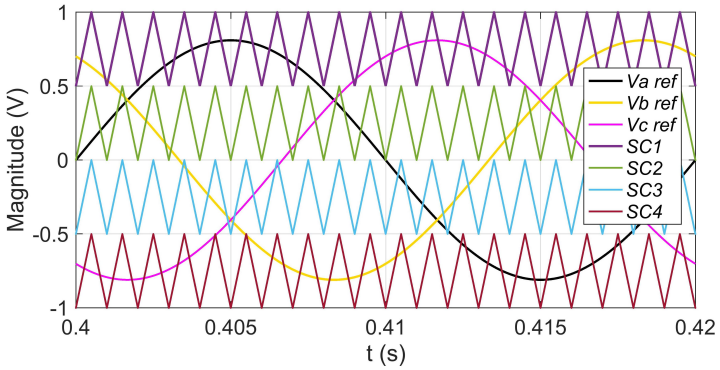

Fig. 5. Five-level switching modulation (PD_SPWM)

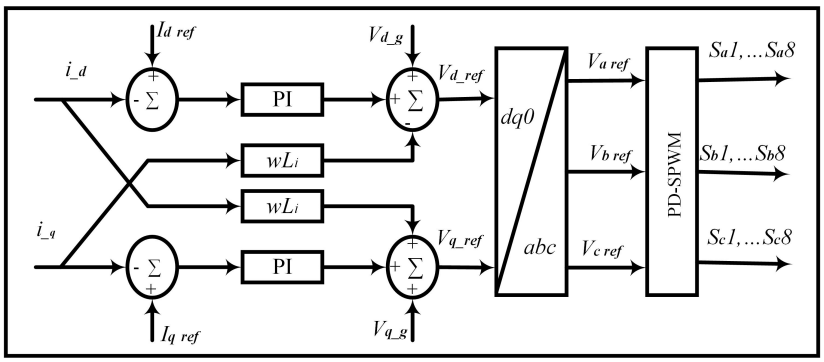

Fig. 6. Block diagram of decoupled vector control

Proportional and integral (PI) parameter gains ($K_p' = 10$ and $K_i' = 4000$) are calculated using (13) and (14)

$$V_{d\_\mathrm{ref}} = (I_{d\mathrm{ref}} - i\_d)\left(K_p' + \frac{K_i'}{s}\right) - wL_i i\_q + V_{d\_g} \tag{13}$$

$$V_{q\_\mathrm{ref}} = (I_{q\mathrm{ref}} - i\_q)\left(K_p' + \frac{K_i'}{s}\right) + wL_i i\_d + V_{d\_g}, \tag{14}$$

where $V_{q\_\mathrm{ref}} = 0$, $V_{d\_\mathrm{ref}} = \sqrt{(2)} \cdot 230$, $I_{q\_\mathrm{ref}} = 0$, and $I_{d\mathrm{ref}}$ value is presented as step variation where initial value is 50 A and final value is 40 A, the step time is 1 s.

2.5. Coupling inductor

The five-level NPC inverter is connected to the grid using the inverter_side inductance (Inductor L_i = 3.5 mH), which is calculated [17] by using the following (15).

$$L_i = \frac{0.1U^2}{2\pi f_c P}, \tag{15}$$

where U is the grid's RMS voltage value (line to line).

The initial conditions of the system and the calculated L_i parameter are listed in Table 5.

Table 5. Initial parameters of (10)

Symbol	Quantity	Value
V_t	The Dc-link voltage of the Output ZSI	800 V
V_g	The grid voltage (RMS: line to ground)	230 V distorted
P	The power MPPT	42.640 kW
f	The fundamental-frequency	50 Hz
f_c	The carrier-frequency	1 kHz

3. Dual Second Order Generalized Integrator technique

When a three-phase/signal phase inverter is coupled to the grid, the continuation of the phase angle of the grid voltage through a Phase Lock Loop (PLL) is critical, as a result, many PLL techniques, such as the DSOGI_PLL, Cascaded Delayed Signal Cancellation (CDSC)_PLL and Multiple Delayed Signal Cancellation (MDSC)_PLL are used for the three-phase /signal phase inverter [18]. The DSOGI_PLL has become one of the most attractive PLL applications because of its simple implementation and great filtering capability. However, most of the existing literature focuses on the structure of the DSOGI and lacks quantitative analysis of the influence of DSOGI on the overall frequency characteristics of the PLL [28].

The DSOGI_PLL is designed to pre-filter (V'_α, V'_β) components using two quadrature-signal-generators (QSGs) that act as a Band-Pass-Filter (BPF) [20]. Besides that, by Quadratic-Signal-Generators (QSGs), it is able to conserve information from positive sequenced harmonics by cancelling negative sequenced harmonics (extracting the positive sequence voltage components $V(_{\alpha,\beta})^+$ in the $\alpha - \beta$ frame (PSC)) [21], then V^+_α and V^+_β are transformed in $V(_{d,q})$ components, which further can be passed to the SRF-PLL for phase estimation and frequency using the Low-Pass-Filter (LPF), the parameters of this filter are set (natural frequency f_n = 5 Hz, and the damping ratio Zeta = 0.707). The block diagram structure of the three-phase DSOGI_PLL is presented in Fig. 7.

As shown in Fig. 7, the block structure of the DSOGI_PLL consists of three essential parts: Dual SGI-QSG, PSC and SRF-PLL.

The SOGI-QSG is based on a Band-Pass-Filter tuned at a resonance angular frequency (center frequency) w' and a damping factor, respectively (quality factor) k, its value is 0.8. There are two main particularities on this filter: one is that it presents at the center frequency two outputs

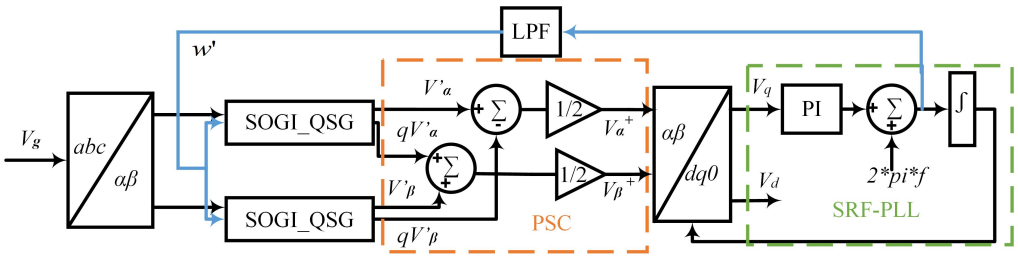

Fig. 7. Block diagram structure of three-phase DSOGI_PLL

with unitary gain, the second is that it allows one to adapt the center frequency. Hence, at the center frequency [29], the voltage signals generated by $D(s)$ and $Q(s)$ are orthogonal (90°), where $D(s)$ is a Band-Pass-Filter (BPF) and $Q(s)$ is a Low-Pass-Filter (LPF). Such behavior can be further comprehended by examining the filter block diagram in Fig. 8. The SOGI-QSG generates the direct and quadrature signals of the input filtered signal. Such behavior can be further understood by analyzing the filter block diagram of Fig. 8 and the transfer functions (16) and (17).

$$D(s) = \frac{V'}{V}(s) = \frac{kw's}{s^2 + kw's + w'^2,} \tag{16}$$

$$Q(s) = \frac{qV'}{V}(s) = \frac{kw'^2}{s^2 + kw's + w'^2}. \tag{17}$$

As shown in Fig. 8, the DSOGI consists of two SOGI-QSGI (one for each component of the Clarke transform), which allows extracting the positive sequence of the three-phase voltage through the positive sequence calculator (PSC) (20), where $qV\alpha'$ and $qV\beta'$ are obtained via the two different SOGI-QSG presented.

$$\begin{cases} V^+_{abc} = T_p V^+_{abc} \quad T_P = \dfrac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \\ V^-_{abc} = T_n V^-_{abc} \quad T_P = \dfrac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \end{cases} \quad a = e^{j\frac{\pi}{2}}, \tag{18}$$

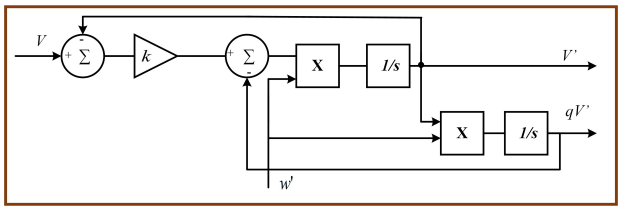

Fig. 8. Block diagram of the SOGI-QSG

$$\begin{cases} V^{+}_{abc} = \left[T_{\alpha\beta}\right] V^{+}_{abc} \\ V^{-}_{abc} = \left[T_{\alpha\beta}\right] \left[T_{p}\right] V^{+}_{abc} \end{cases}, \tag{19}$$

$$\begin{bmatrix} V^{+}_{\alpha} \\ V^{+}_{\beta} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1-q \\ q \end{bmatrix} \begin{bmatrix} V'_{\alpha} \\ V'_{\beta} \end{bmatrix} q = e^{-j\frac{\pi}{2}}. \tag{20}$$

The SRF-PLL part of the global structure of the three-phase DSOGI_PLL is employed to achieve phase-locking by closed loop control of V_q voltage component, its PI parameters (K''_p and K''_i) are synthesized in (21).

$$K''_p = \frac{\hat{V}g}{4\xi^2}, \quad K''_i = \frac{2w_n\xi}{\hat{V}g}, \tag{21}$$

where: w_n represents the filter natural frequency, $\dfrac{\hat{V}g}{4\xi^2}$ is the grid peak voltage amplitude, and ζ is the damping. After calculating, the values for the PI control gain are: $K''_p = 10$ and $K''_i = 30$.

4. Simulation results and discussions

The simulation of the proposed system is made under MATLAB_SIMULINK environments. The results of the DC input-output of the Z-Source voltage, currents, active and reactive power, voltage waveforms, and THD(i) of current analysis are discussed in this section. Those results are given to confirm the suggested structure's quality; the circuit parameters are summarized in Tables 2 and 5.

4.1. Output DC voltage of ZSI

The Z-Source network parameters are $L1 = L2 = 8$ mH and $C1 = C2 = 50$ µF.

As shown in the simulation results (Fig. 9), there is a direct relationship between the values of the DC output voltage ($2V_{\mathrm{Output}ZS}$) and its DC input voltage (4PV source voltage).

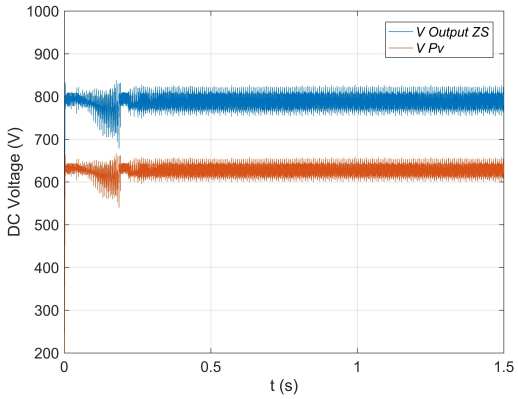

Fig. 9. Output DC-link voltage of the ZS and DC voltage of PV source (V_{PV})

Those values are proportional: $V_{\text{OutputZS}} = B \cdot (2V_{\text{PV}})$, where B is the boost factor and roughly equals the value 1.2; on the other hand, V_{PV} is boosted by around 800 V, perfectly matching the theoretical value $B = 1.26$.

4.2. Output voltage of the five-level inverter

Figure 10 shows the waveform of the three-phase voltage of the five-level NPC inverter. This topology operates under the condition of $f = 50$ Hz, the inverter's control is PD-SPWM, and the modulation index is set to $M = 0.81$.

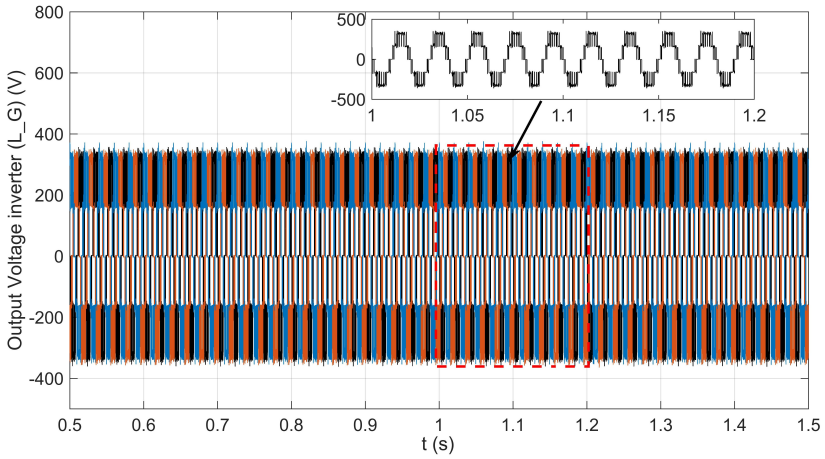

Fig. 10. Output voltage inverter

As shown in Fig. 10, the inverter output voltage phase has an almost sinusoidal form; therefore, the quality of the voltage waveform is proportional to the level of the inverter (that it appears more like a sine wave as the number of levels increases), and the AC value's peak voltage $v\hat{O}x$ is approximately 324 V $\approx \sqrt{(2)} \cdot 230$ V, and it is validated by (7).

4.3. Grid voltage in $\alpha - \beta$ frame, phase, angular frequency, and frequency estimation of DSOGI_PLL

The results related to grid voltage in alpha-beta ($\alpha - \beta$) frame, phase, angular frequency, and frequency are optimized by the DSOGI_PLL method, which has been applied to the distorted grid (as shown in Fig. 11) and are presented in Figs. 12, 13, and 14.

As illustrated in Fig. 11, a typical voltage variation due to harmonic distortion (programmed grid) used in our simulation is characterized by its voltage THD(v) = 7.45%, the non-sinusoidal waveform, and the peak value of each voltage is more than 565.7 V (the peak value voltage in the synchronization case; line to line).

As illustrated in Figs. 12, 13, and 14, the use of the DSOGI_PLL technique with filter is the preferable option for the generation of orthogonal signals. These are identical magnitudes with a 90° phase displacement between the direct and quadratic components of the grid voltage, and this control can estimate the phase accurately under various conditions (harmonic distortion).

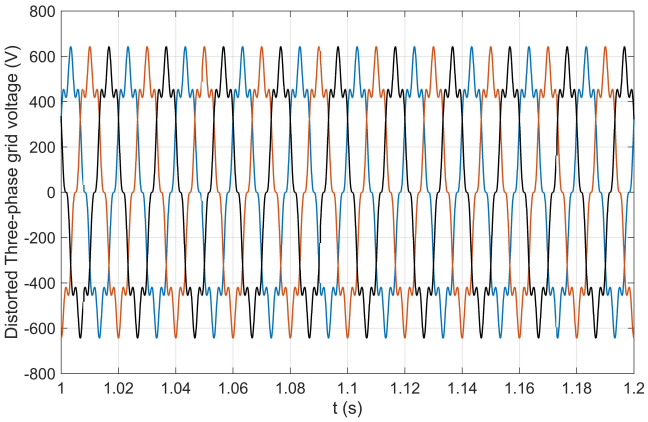

Fig. 11. Distorted three-phase grid voltage (line to line)

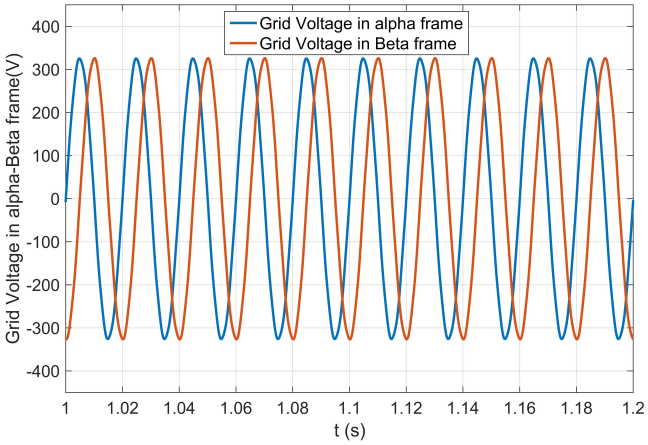

Fig. 12. Grid voltage in $\alpha - \beta$ frame and estimation of DSOGI_PLL

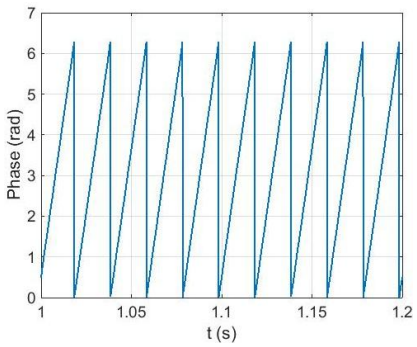

Fig. 13. Phase estimation of DSOGI_PLL

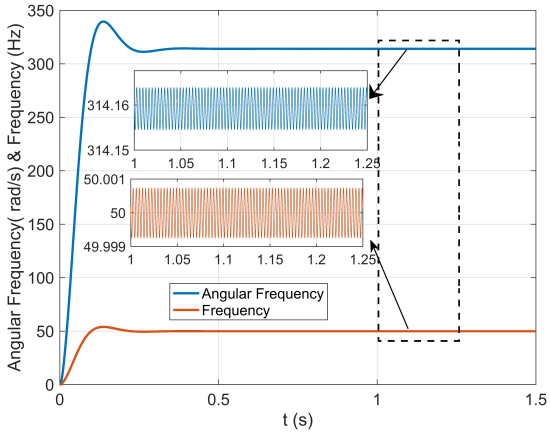

Fig. 14. Angular frequency and frequency estimation of DSOGI

Figure 14 shows the angular frequency and estimated frequency by this technique. In the time band $t = [1, 1.2]$, we have found that there is a small oscillation of very less magnitude in the detected frequency and angular frequency around ±0.001 (Hz) and ±0.005 (rad/s), respectively. These values are very negligible, and the results obtained are similar to the synchronized grid case.

4.4. Current controller

The objective of changing the current values is to test the robustness of the control method against variable conditions. We apply a step form of the current (I_{dref}), which changes from 50 A (between 0 s and 1 s) to 40 A (between 1 s and 1.5 s), where Id ref is the reference current in the (dq) frame.

The peak value of the output current after filtering i_{Ox} ($x = a, b$ or c) follows perfectly its reference, as shown in Figs. 15 and 17, the maximum value of the inverter output current i_{Ox} equals I_d.

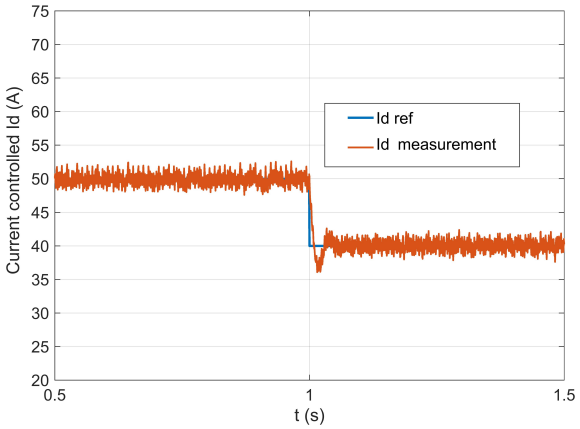

Fig. 15. Current (I_d) with referenced current

Figure 16 shows that the active power has the same behavior as the current, furthermore, the controlled system behaves with a very short response time when a sudden reference change is applied. Also, our control totally compensates for the reactive power; it joints 0 var all the simulation time period, as shown in Fig. 16.

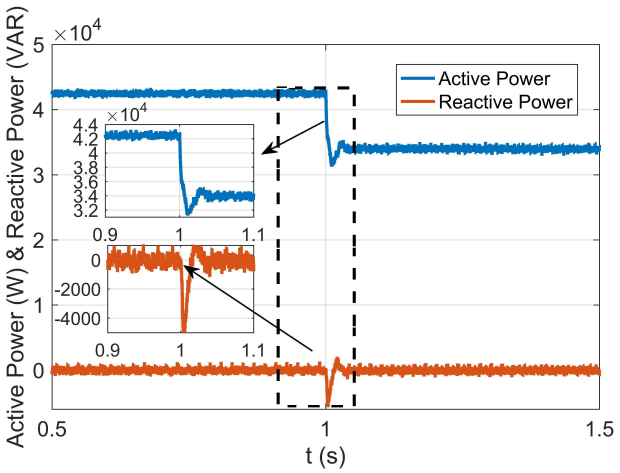

Fig. 16. Active and reactive power

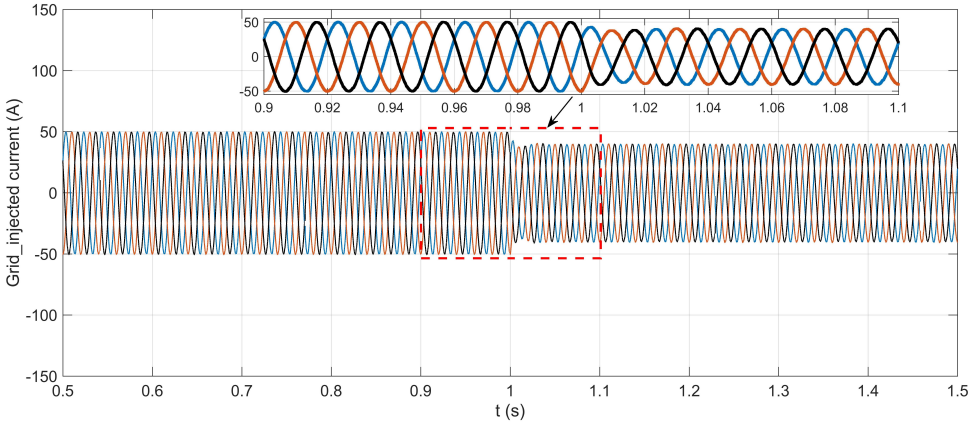

Fig. 17. Grid_injected courant $I_d = [50, 40]$ (A)

The THD of the grid-injected current is clearly accepted (for $I_{d\text{ref}} = 50$ A, the THD = 0.96%, and for $I_{d\text{ref}} = 40$ A, the THD = 1.20%), as illustrated in Figs. 18, and 19.

It has been observed from the FFT analysis of the grid-injected current and the fundamental harmonic THD that when the reference current is 50 A, the THD is 0.96%. When the reference current decreases to 40 A, the THD increases to 1.2%, so there is an inverse relationship between the current's values and the THD ($I_{d\text{ref}} \uparrow$ the THD$\downarrow$). In our results, THD values are very low, less than 5%. These results also show that the PV energy integrated into the grid is of high quality.

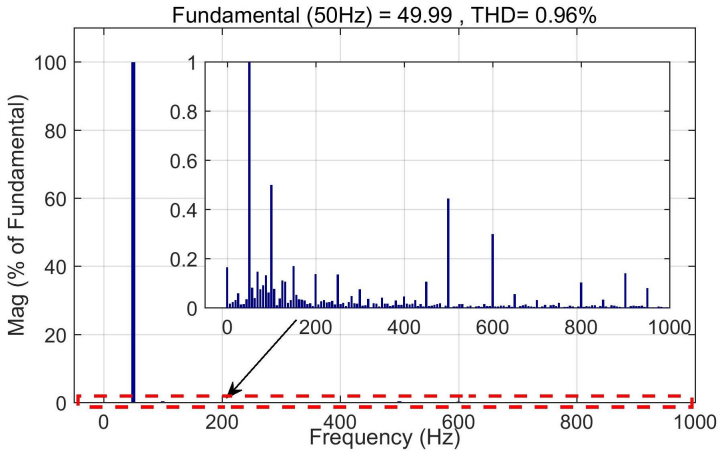

Fig. 18. THD of the current controlled $I_d = 50$ (A)

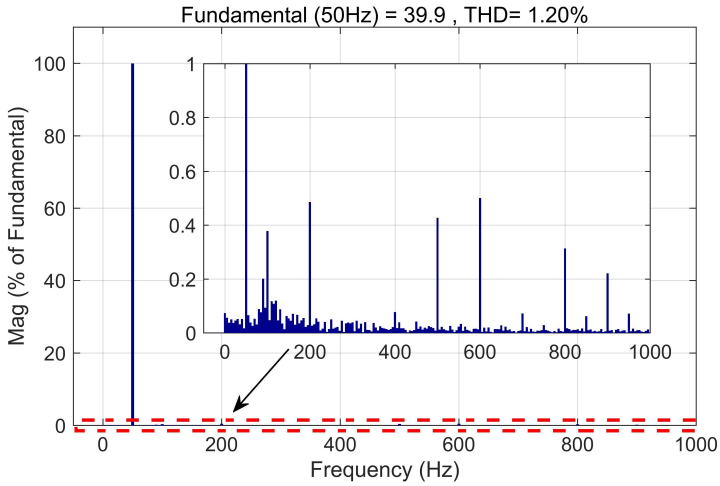

Fig. 19. THD of the current controlled $I_d = 40$ (A)

5. Conclusion

The DSOGI_PLL technique is used to synchronize the connection of a PV system to a distorted power grid through a Z-Source NPC five-level inverter is presented in this article.

The configuration of the proposed system is designed and simulated using MATLAB/Simulink.

As it turns out, the performance of DSOGI_PLL control with LPF is more efficient in phase and frequency estimation of grid voltage under various conditions (distorted grid), and the results show that ripples are clearly minimized.

The use of the Z-Source technique allows us to eliminate the DC bus with its control, as well as the use of the DC-DC Boost converter as an intermediary. Also, Z-Source is used to increase the PV voltage; without any control system, this augmentation is related to the ZSI parameters ($L1, L2, C1, C2$) and the Carrier-frequency (f_c).

NPC five-level inverter presents several benefits, such as the generation of high-quality currents as well as the capacity to operate at a lower switching frequency than a two-level or three-level inverter. The grid current total harmonic distortion (THD) is remarkably reduced by 0.96% and 1.2% in our case compared to 5% in IEC 61000-3-2 and IEEE-519 standards, and there is an inverse relationship between the reference current and its value's THD.

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