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Active disturbance rejection and current sharing control of six-phase interleaved parallel synchronous buck converters with high dynamic response

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Abstract:

Unmanned Aerial Vehicle (UAV) frequently encounter various external disturbances during flight. After experiencing such disturbances, the UAV's power supply must quickly respond and maintain stable output. To address this problem, this paper proposes an improved active disturbance rejection control (IADRC) scheme combined with peak current mode control (PCMC) based on a six-phase interleaved parallel synchronous buck converter. Modal analysis was conducted on the synchronous buck converter, and small-signal modeling was performed under current control mode to analyze closed-loop stability. The dynamic response speed was improved by utilizing a peak current inner loop, enabling precise current sharing. The system's disturbance rejection capability was enhanced by employing an improved extended state observer for real-time estimation of disturbances. This approach offers advantages such as high dynamics, strong disturbance rejection, and good current sharing. Finally, an experimental prototype with a rated power of 1000 W, maximum efficiency of 96.9%, and power density of 12.9 W/cm^2 was constructed. Comparing three different control schemes, the response waveforms of the prototype verify the feasibility and advancement of the scheme in this paper.

Key words: active disturbance rejection control (ADRC), current sharing control, dynamic response, peak current control, synchronous buck converter

1. Introduction

In recent years, with the rapid development of Unmanned Aerial Vehicle (UAV) technology, these multi-rotor vehicles have become the center of attention in various fields. UAVs are not only widely used in aerial photography to document life, but also play an important role in UAV

shows for commercial events and military reconnaissance operations. However, this wide range of applications has also increased the demands on UAV power supplies, requiring higher power density, greater efficiency, and faster dynamic response [1–3]. The design of UAV power supplies has become increasingly challenging as they must deliver sufficient power within a confined space while also addressing the potential for frequent disturbances to the aft servos during flight. These characteristics place certain limitations on traditional power management solutions.

In order to solve the above problems, the researchers selected the polyphase interleaved parallel BUCK converter as the power module for the UAV and conducted a lot of research on it. In the existing scientific research [4], a high-power, high-voltage four-phase interleaved buck converter is designed, and a control strategy based on PI and maximum equalization control is proposed, which better realizes the high-power output and equalization. However, the designed converter is large in size and is unsuitable to unmanned aircraft systems. In [5], a decentralized control strategy is proposed. Through accurate modeling, the commonly used droop control algorithm in grid-connected inverters is integrated into a five-phase interleaved parallel buck converter. This achieves the effects of current equalization and interference immunity without the need for additional communication. However, the modeling process is complex, and the control difficulty is high. It may not be suitable for UAV power control requiring high reliability. In [6], dynamic performance by reducing the size and output ripple by merging the discrete inductors in the circuit into coupled inductors and improving the voltage-current double closed-loop control. However, due to the characteristics of average current control, the system response speed still cannot be greatly improved. leaving room for improvement in systems that require high dynamics.In [7–10] explores the use of robust controllers that achieve good immunity, but none of them improve the fastness of the system.

In [11], a novel Lyapunov's control method for multiphase DC–DC converters is proposed, which improves dynamic response speed and simplifies implementation by reducing the number of integrators. However, it does not enhance disturbance rejection compared to conventional PI control. In [12], a framework that simplifies control design for multilevel DC–DC converters by extending the common quadratic Lyapunov function (CQLF) is approached. This method demonstrates fast dynamic response and good load disturbance rejection. However, it still requires complex nonlinear optimization and is limited by its focus on specific converter types. Further research and broader testing are needed to address these limitations. In [13–15], a method is proposed to apply Dynamic Voltage Restoration (DVR) to multi-phase interleaved parallel DC–DC converters. Experimental results showed that it can effectively improve the dynamic performance of the system, but it requires additional components. In [16], a discrete-time integral sliding mode observer (DISMO) predictive controller is proposed. The dynamic performance of the proposed DISMO-based predictive controller is better than the PI controller under different scenarios. However, the results are limited to simulation and further experiments have not been conducted. In [17], an optimized MPC control is applied to a single-phase BOOST PFC. This method effectively optimizes the dynamic response and THD performance, but still requires large computational resources and it remains to be demonstrated whether it can be applied to other converters. In [18–20], improved model-free control has been used to increase system speed and robustness. However, these methods involve excessive computational complexity, making them difficult to apply in practical engineering scenarios.

The research indicates that while advanced control methods can improve both dynamic response and disturbance rejection in converters, many algorithms either cannot optimize both or are too complex to implement. Therefore, developing a simple and effective algorithm to optimize both aspects is crucial for UAV power systems.

To better address the need for UAV power supplies. In this paper, an Improved Active Disturbance Rejection Control (IADRC) algorithm combined with Peak Current Mode Control (PCMC) is proposed. It significantly enhances the dynamic capabilities and disturbance resilience of UAV power systems with simple design process that is easy to implement. This innovation is particularly advantageous for applications requiring high dynamic performance and disturbance rejection, such as unmanned aerial vehicles. The remainder of the paper is organized as follows: Section 2 provides a brief introduction to the topology structure and its operating principles. Section 3 analyses the modes under different duty cycles using a dual interleaved parallel buck converter as an example. In Section 4, the basic principles of peak voltage regulation and small signal models are explained, and the control strategy of this paper is proposed. Section 5 describes the experimental platform setup and provides experimental validation. The superiority of the proposed control approach is demonstrated by comparison with several traditional control methods. Finally, conclusions are given in Section 6.

2. Topology structure and based principle

Figure 1 illustrates the topology of an N-phase interleaved parallel synchronous buck converter.

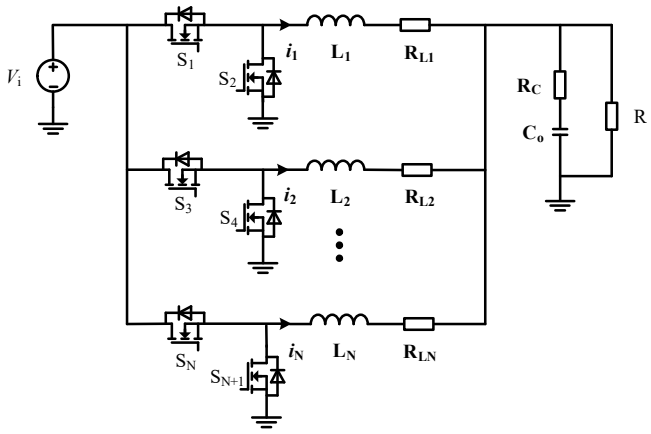

Fig. 1. N-phase interleaved parallel synchronous buck converter

This topology consists of multiple synchronous buck converters connected in parallel, where all the freewheeling diodes are replaced by power switching MOSFETs. When freewheeling diodes are necessary, the MOSFETs, functioning as diodes, turn on synchronously. This reduces conduction losses and enhances the overall efficiency of the circuit.

Similar to single-phase synchronous buck converters, interleaved parallel buck converters use the energy storage properties of electronic components such as inductors and capacitors to transfer energy from the input side to the load side to achieve voltage conversion.

3. Interleaved parallel synchronous buck mode analysis

When the interleaved parallel synchronous buck operates in different duty cycle ranges, its modes vary accordingly. To analyze these modes, this paper examines a two-phase interleaved parallel synchronous buck converter as a case study across various duty cycle ranges. Ultimately, the paper derives the expression for the output current ripple of an N-phase interleaved parallel synchronous buck converter.

3.1. 0 < D < 1/2

When the two interleaved parallel synchronization buck is in the duty cycle $0 < D < 1/2$, as shown in Fig. 2, there is no overlapping of the duty cycle. Define S_x to represent the conduction of the upper switch in the x-th channel. $\overline{S}_x$ to represent the shutdown of the upper switch in the x-th channel, so there are three modes in this duty cycle range respectively $S_1\overline{S}_2$, $\overline{S}_1S_2$, $\overline{S}_1\overline{S}_2$, as shown in Fig. 3.

When in the *Mode* $S_1\overline{S}_2$, where the upper switch of one phase is on, the power source charges inductor L_1 from the input capacitor C_i, simultaneously providing energy to the load. At this time, the inductor current i_1 linearly increases. The lower switch of the second phase is on, causing the inductor to discharge, resulting in the linear decrease of the inductor current i_2. From this, we can derive the state Eq. (1).

$$\begin{cases} \dfrac{\mathrm{d}i_1}{\mathrm{d}t} = \dfrac{V_i - V_o}{L_1} = \dfrac{V_i \cdot (1-D)}{L_1} \\ \dfrac{\mathrm{d}i_2}{\mathrm{d}t} = \dfrac{0 - V_o}{L_2} = -\dfrac{D \cdot V_i}{L_2} \\ \dfrac{\mathrm{d}V_c}{\mathrm{d}t} = \dfrac{R \cdot (i_1 + i_2) - V_o}{R \cdot C} \end{cases} . \tag{1}$$

In *Mode* $\overline{S}_1\overline{S}_2$, both upper switches of the two phases are turned off simultaneously, while both lower switches are turned on. At this point, the inductor currents i_1 and i_2 decrease linearly. The state Eq. (2) for this mode can be derived.

$$\begin{cases} \dfrac{\mathrm{d}i_1}{\mathrm{d}t} = \dfrac{0 - V_o}{L_1} = -\dfrac{D \cdot V_i}{L_1} \\ \dfrac{\mathrm{d}i_2}{\mathrm{d}t} = \dfrac{0 - V_o}{L_2} = -\dfrac{D \cdot V_i}{L_2} \\ \dfrac{\mathrm{d}V_c}{\mathrm{d}t} = \dfrac{R \cdot (i_1 + i_2) - V_o}{R \cdot C} \end{cases} . \tag{2}$$

In *Mode* $\overline{S}_1S_2$, one upper switch is turned off while the other is turned on. At this moment, the inductor currents i_1 and i_2 have opposite directions of change compared to the inductor currents in mode $S_1\overline{S}_2$. Similarly, the state Eq. (3) for this mode can be derived.

$$\begin{cases} \dfrac{\mathrm{d}i_1}{\mathrm{d}t} = \dfrac{0 - V_o}{L_1} = -\dfrac{D \cdot V_i}{L_1} \\ \dfrac{\mathrm{d}i_2}{\mathrm{d}t} = \dfrac{V_i - V_o}{L_2} = \dfrac{V_i \cdot (1 - D)}{L_2} \\ \dfrac{\mathrm{d}V_c}{\mathrm{d}t} = \dfrac{R \cdot (i_1 + i_2) - V_o}{R \cdot C} \end{cases} . \tag{3}$$

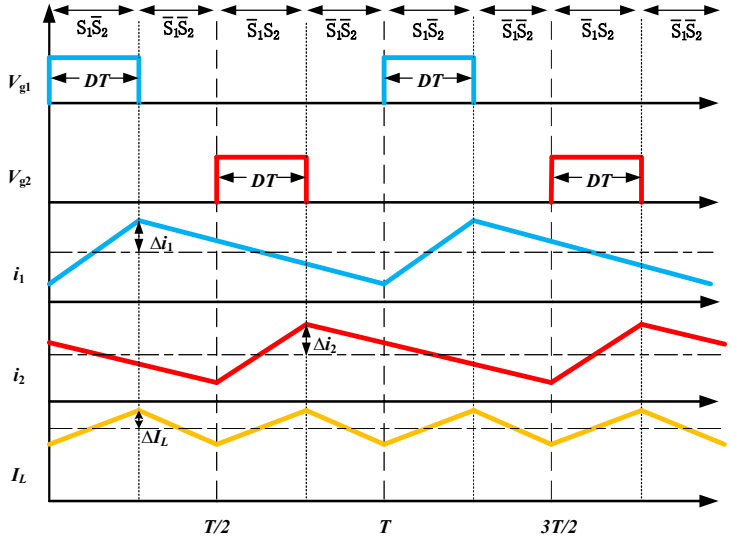

Fig. 2. The relationship between the driving signals and the inductor currents when $0 < D < 1/2$

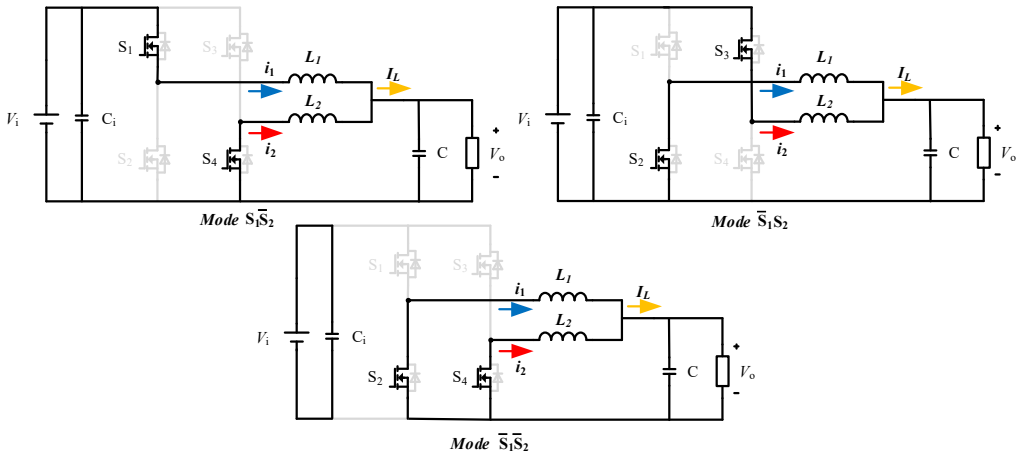

Fig. 3. The mode of $0 < D < 1/2$

In *Mode* $S_1\overline{S}_2$, the expression for the inductor current ripple can be derived from Eq. (1), resulting in Eq. (4):

$$\Delta i_1 = \frac{V_i \cdot (1-D)}{L_1} \cdot DT, \quad \Delta i_2 = -\frac{D \cdot V_i}{L_2} \cdot DT. \tag{4}$$

The total output current ripple ΔI_L is equal to the sum of the inductor current ripples Δi_1 and Δi_2. In the ideal case where L_1 equals L_2 and $D = V_o/V_i$, then ΔI_L is:

$$\Delta I_L = \frac{V_i \cdot [L_2(1-D) - L_1 D] \cdot DT}{L_1 L_2} = \frac{(V_i - 2V_o)DT}{L}. \tag{5}$$

The inductor current ripple for *Mode* $\overline{S}_1\overline{S}_2$ and the total output current ripple can be derived from Eq. (2)

$$\Delta i_1 = -\frac{D \cdot V_i}{L_1} \cdot \left(\frac{1}{2} - D\right) T = \Delta i_2, \tag{6}$$

$$\Delta I_L = -\frac{(V_i - 2V_o)DT}{L}. \tag{7}$$

The inductor current ripple for *Mode* $\overline{S}_1 S_2$ and the total output current ripple can similarly be derived from Eq. (3):

$$\Delta i_1 = -\frac{D \cdot V_i}{L_2} \cdot DT, \quad \Delta i_2 = \frac{V_i \cdot (1-D)}{L_1} \cdot DT, \tag{8}$$

$$\Delta I_L = \frac{(V_i - 2V_o)DT}{L}. \tag{9}$$

3.2. 1/2 < *D* < 1

When the synchronous buck converter operates with a duty cycle of $1/2 < D < 1$, compared to the duty cycle of $0 < D < 1/2$, the *Mode* $\overline{S}_1\overline{S}_2$ is reduced, but a new *Mode* $S_1 S_2$ is added, as shown in Fig. 4.

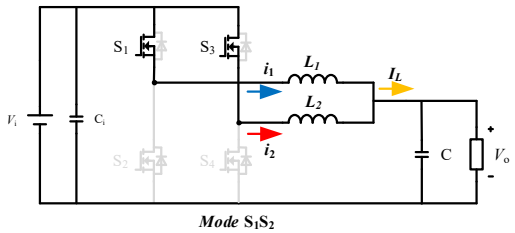

Fig. 4. The additional mode introduced when $1/2 < D < 1$

In *Mode* S_1S_2, both switches on paths one and two conduct simultaneously, and the inductor currents rise linearly with the same slope. This can be expressed as its state Eq. (10).

$$\begin{cases} \dfrac{\mathrm{d}i_1}{\mathrm{d}t} = \dfrac{V_i - V_o}{L_1} = \dfrac{V_i \cdot (1-D)}{L_1} \\ \dfrac{\mathrm{d}i_2}{\mathrm{d}t} = \dfrac{V_i - V_o}{L_2} = \dfrac{V_i \cdot (1-D)}{L_2} \\ \dfrac{\mathrm{d}V_c}{\mathrm{d}t} = \dfrac{R \cdot (i_1 + i_2) - V_o}{R \cdot C} \end{cases}. \tag{10}$$

Figure 5 shows the relationship between the inductor current and the switch signals when the duty cycle is $1/2 < D < 1$.

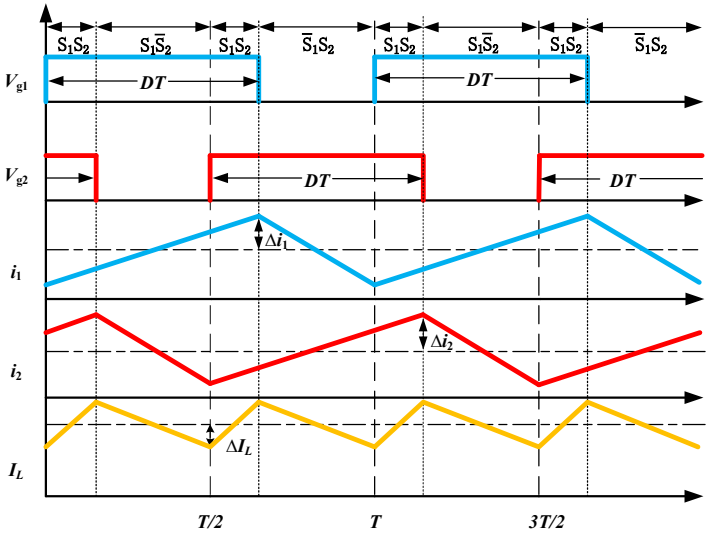

Fig. 5. The relationship between the driving signals and the inductor currents when $1/2 < D < 1$

Upon entering *Mode* S_1S_2, the expressions for the inductor current and the output current ripple can be derived using Eq. (10), with the resulting expressions provided in Eqs. (11) and (12).

$$\Delta i_1 = \frac{V_i \cdot (1-D)}{L_1} \cdot \left(D - \frac{1}{2}\right) T = \Delta i_2, \tag{11}$$

$$\Delta I_L = \frac{(2V_i - 2V_o)\left(D - \frac{1}{2}\right) T}{L}. \tag{12}$$

In summary, the expression for the output current ripple of a two-phase interleaved parallel buck converter can be derived.

$$|\Delta I_L| = \begin{cases} \dfrac{1-2D}{1-D} \Delta I_i & (0 < D < 1/2) \\ \dfrac{2D-1}{D} \Delta I_i & (1/2 < D < 1) \end{cases}. \tag{13}$$

ΔI_i represents the output current ripple of a single-phase buck converter. From this, the output current ripple expression for an N-phase parallel buck converter can also be derived.

$$|\Delta I_L| = \frac{(n - ND)(ND - n + 1)}{(1 - D)ND} \Delta I_i, \tag{14}$$

where N represents the number of parallel branches, and n denotes the n-th segment when the duty cycle D is divided into N segments. From Eq. (14), it can be observed that, for a fixed duty cycle, increasing the number of interleaved parallel branches results in a reduction of the output current ripple. However, in practice, factors such as current sharing, heating, power density, etc. must be considered. Taking these factors into consideration, a six-phase interleaved parallel buck converter is selected as the power supply topology in this paper.

4. Control strategy design

In this paper, the control strategy adopts an improved active disturbance rejection controller combined with peak current mode control (PCMC-IADRC), where the control loop mainly consists of an improved active disturbance rejection voltage outer loop and a peak current inner loop. PCMC-IADRC demonstrates faster response speed and better disturbance rejection capability than traditional PI voltage-current dual loop control, while maintaining comparable steady-state performance. This makes it better suited to the requirements of UAV power systems.

4.1. Peak current control and small-signal model

4.1.1. The principle of peak current control

Conventional control modes include voltage control mode and current control mode. Peak current control offers faster dynamic response speed, inherent current limiting effect, simplified control loop design, and the capability to achieve automatic current sharing compared to voltage control mode. However, peak current control systems may encounter open-loop instability and subharmonic oscillations when the duty cycle exceeds 50%. To address this issue, slope compensation is typically required. In this control mode, the system is sensitive to noise, and its disturbance rejection capability is relatively weak. Figure 6 shows the block diagram of peak current control for a synchronous buck DC–DC converter. Where R_i is the current sampling resistor, G_{mEA} is the transfer function of the voltage outer loop, and V_{EA} is the output value of the voltage outer loop.

4.1.2. Small-signal modeling of peak current control

The synchronous buck converter is a time-varying nonlinear system with two switch modes. Due to the complexity of direct stability analysis, many scholars have conducted extensive research on current control modeling. The most classic and widely used model is Dr. Raymond Ridley's peak current small-signal model. The paper cites its conclusions due to the complexity of the modeling process and difficulty in analysis. The accuracy of the model can reach half of the switching frequency [21, 22].

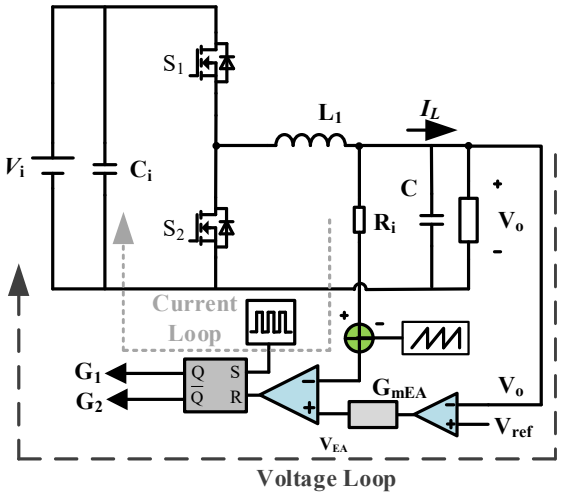

Fig. 6. Peak current control block diagram

The small-signal model of peak current control is depicted in Fig. 8, where the dashed lines represent the equivalent model of the PWM switch. Small-signal disturbances of the duty cycle and input voltage are represented by $\hat{d}$ and $\hat{v}_g$ respectively. The current sensing transfer function is denoted by $He(s)$, while Fm represents the small-signal model of duty cycle modulation. The small-signal model of the current inner loop input is represented by $\hat{v}_{\mathrm{EA}}$, and k_f and k_r are the gains corresponding to the input and output small signals, respectively. S_e represents the slope of the slope compensation, and S_n represents the slope of the inductor current. Previous literature suggests that:

$$G(s) = \frac{\hat{v}_o(s)}{\hat{v}_{\mathrm{EA}}(s)} \approx F_g(s) * F_p(s) * F_k(s), \tag{15}$$

$$F_g(s) = \frac{R}{R_i} \cdot \frac{1}{1 + \dfrac{R \cdot T}{L} M}, \tag{16}$$

$$F_p(s) = \frac{1 + sR_{\mathrm{ESR}}C}{1 + s\left(\dfrac{LRC}{L + MRT}\right)}, \tag{17}$$

$$F_k = \frac{1}{1 + \dfrac{s\pi M}{w_n} + \dfrac{s^2}{w_n^2}}, \tag{18}$$

$$M = \left(1 + \frac{S_e}{S_n}\right)(1 - D) - 0.5. \tag{19}$$

In the current control mode, the inductor is equivalent to a current source controlled by voltage. As a result, the power stage no longer exhibits the characteristics of an LC second-order system, but instead becomes a first-order system. It is important to design the compensation loop accordingly. Figure 7 shows the small signal model for peak current mode.

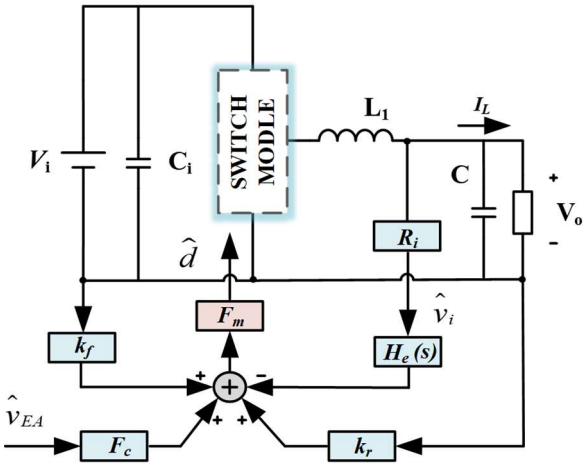

Fig. 7. Peak current control small-signal model

Table 1 presents the primary parameters of the power supply designed in this paper. By substituting these parameters into Eq. (15), the Bode diagram corresponding to the open-loop transfer function can be plotted using MATLAB, as depicted in Fig. 8.

Table 1. Parameters of the six-phase interleaved synchronous buck converter

Parameters	Symbol	Value
Output capacitor	C	600 μF
Input voltage	V_i	60 V
Output voltage	V_o	28.5 V
Inductor	L	13 μH
Sampling resistor	R_i	3 mΩ
Switch frequency	f_s	150 kH
Capacitor ESR	C_{ESR}	0.03 mΩ
Ratng power	P	1000 W

The Bode plot reveals that the system exhibits a pole at 450 Hz, where the gain slope decreases by –20 dB/dec. At 34.4 kHz, a zero introduced by the capacitor ESR causes the gain to return to 0 dB/decade. Additionally, two high-frequency poles emerge around half of the switching frequency, resulting in a gain slope of –40 dB/dec. Due to the presence of high-frequency poles, the system is stable, but the stability margin is only 20.7° and the crossover frequency is too high, resulting in a slow system response. Consequently, voltage outer loop compensation must be designed to enhance the system's stability margin and response time.

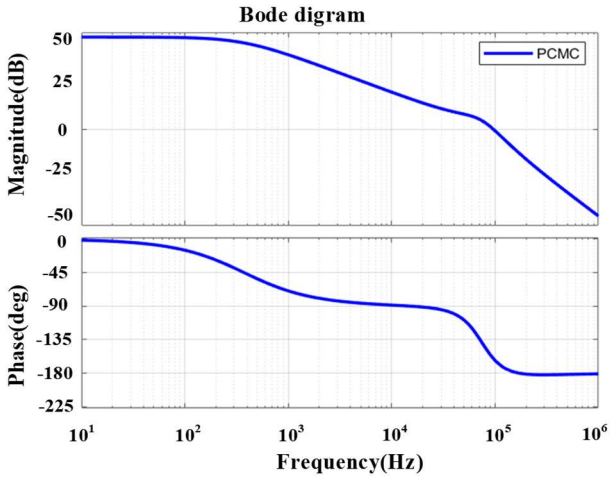

Fig. 8. The uncompensated open-loop Bode plot of the system

4.2. Combining improved active disturbance rejection control with peak current control

ADRC is a control method that actively estimates and compensates for disturbances in the system. It can effectively resist various external, and internal system disturbances, making the control system robust against these disturbances and less susceptible to their effects. Additionally, it can respond rapidly to system disturbances and adjust accordingly, thereby enhancing the system's dynamic performance. ADRC has been widely applied in industrial control and practical engineering [23].

The block diagram illustrating the proposed improved ADRC algorithm integrated with peak current control is depicted in Fig. 9. z_1 and z_2 denote the estimated values of the output voltage U_0 and the total disturbance f through the state observer, while k_p and b_0 represent controller parameters adjustable for refining controller performance. r_1 signifies external disturbances, encompassing load transients and input voltage transients, whereas r_2 denotes internal disturbances, primarily stemming from variations in the duty cycle of the synchronous buck converter.

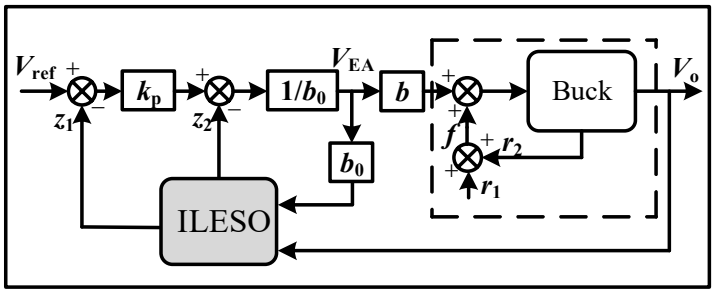

Fig. 9. The block diagram of the improved ADRC

From the ADRC theory, we can derive the expression for the output derivative, as given in Eq. (20).

$$U_o = bV_{\mathrm{EA}} + f(U_o r_1 t), \tag{20}$$

where b represents the gain of the control variable, constituting an inherent parameter of the system.

In practical control systems, accurately estimating the true value of b is unfeasible. Therefore, the estimated value of b is denoted as b_0. By simultaneously adding and subtracting $b_0 V_{\mathrm{EA}}$ on the right side of Eq. (20), and subsequently amalgamating $(b - b_0)V_{\mathrm{EA}}$ into the total disturbance, we can reformulate Eq. (20) as Eq. (21).

$$\begin{aligned} U_o &= bV_{\mathrm{EA}} + bV_{\mathrm{EA}} - bV_{\mathrm{EA}} + f\left(U_o, r_1, t\right), \\ U_o &= bV_{\mathrm{EA}} + (b - b_0)\, V_{\mathrm{EA}} + f\left(U_o, r_1, t\right), \\ U_o &= bV_{\mathrm{EA}} + f\left(U_o, r_1, t\right). \end{aligned} \tag{21}$$

Selecting the state variables $x_1 = U_o$, $x_2 = f$, $h = \dot{f}$:

$$\begin{cases} x = Ax + BV_{\mathrm{EA}} + Eh \\ U_o = Cx + DV_{\mathrm{EA}} \end{cases}, \quad A = \begin{pmatrix} 0 & 1 \\ 0 & 0 \end{pmatrix}, \; B = \begin{pmatrix} b_0 \\ 0 \end{pmatrix}, \; C = \begin{pmatrix} 1 & 0 \end{pmatrix}, \; D = 0, \; E = \begin{pmatrix} 0 \\ 1 \end{pmatrix}. \tag{22}$$

From this, we can construct a linear observer for the synchronous buck converter:

$$\begin{cases} z = \begin{bmatrix} -\beta_1 & 1 \\ -\beta_2 & 0 \end{bmatrix} z + \begin{bmatrix} b_0 & \beta_1 \\ 0 & \beta_2 \end{bmatrix} \begin{bmatrix} V_{\mathrm{EA}} \\ U_o \end{bmatrix} \\ \hat{U}_o = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} z \end{cases}. \tag{23}$$

z_1 will track x_1, and z_2 will track x_2. Consequently, upon system convergence, z_1 will approximate U_o, while z_2 will approximate f. β_1 and β_2 represent the gains of the linear observer, dictating the convergence speed of z_1 and z_2. These two parameters allow for adjustment of the convergence speed. Typically, β_1 and β_2 can be set as follows:

$$\beta_1 = 2\omega \quad \beta_2 = \omega^2. \tag{24}$$

ω denotes the bandwidth of the observer. A higher value of ω enhances the tracking performance of the observer while diminishing its disturbance rejection capability. Hence, it is crucial to strike a balance between tracking performance and disturbance rejection when determining the value of ω.

From Eq. (23), we can obtain the expression for the extended observer in LADRC.

$$\begin{cases} e = U_o - z_1 \\ z_1 = z_2 + b_0 V_{\mathrm{EA}} + \beta_1 e \\ z_2 = \beta_2 e \end{cases}. \tag{25}$$

e represents the observation error of ESO. From Fig. 10, the expression for V_{EA} can be deduced.

$$V_{\mathrm{EA}} = \frac{k_p(U_{\mathrm{ref}} - z_1) - z_2}{b_o}. \tag{26}$$

Substituting Eq. (26) into Eq. (25) and simplifying, we can derive the transfer function of the traditional first-order ADRC compensator.

$$G_c(s) = \frac{(\beta_2 + \beta_1 k_p)s + \beta_2 k_p}{b_0 s^2 + (b_0\beta_1 + b_0 k_p)s}. \tag{27}$$

The first-order observer structure can be illustrated based on Eqs. (23) and (25), as shown in Fig. 10.

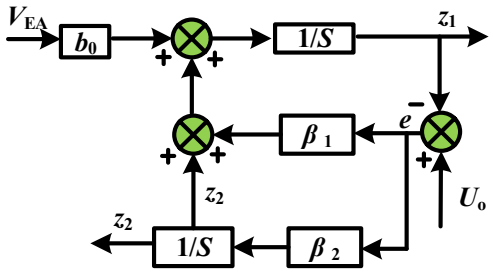

Fig. 10. The structure diagram of the first-order linear observer

In order to bolster the disturbance rejection capability of the ADRC, the Linear Extended State Observer (LESO) is improved in this paper. By incorporating an error proportional-integral loop and a second-order low-pass filter, the system's performance was improved. This enhancement maintains a rapid response while increasing the system's capability to reject disturbances. The improved linear observer diagram is depicted in Fig. 11.

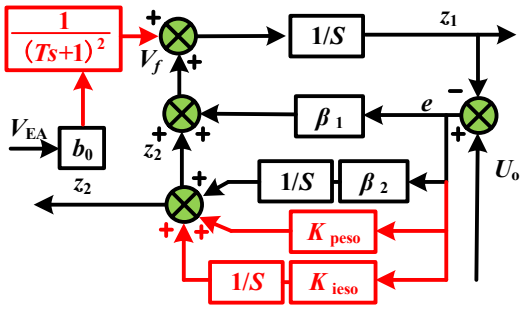

Fig. 11. The improved first-order linear state observer

The expression for the improved linear observer can be written as:

$$\begin{cases} e = U_o - z_1 \\ z_1 = \dfrac{(z_2 + b_o V_{EA} H + \beta_1 e)}{s} \\ z_2 = \dfrac{(\beta_1 + K_{ieso})\, e}{s} + K_{peso} e \\ H = \dfrac{1}{(Ts+1)^2} \end{cases}. \tag{28}$$

Substituting Eq. (26) into Eq. (28) yields the expression for the improved first-order linear ADRC compensator:

$$G_c'(s) = \frac{K_{\text{peso}}s^2 + (\beta_2 + K_{\text{ieso}} + \beta_1 k_p + K_{\text{peso}}k_p)s + k_p\beta_2 + K_{\text{ieso}}k_p}{b_0[s^2 + (k_p - K_{\text{peso}})Hs + (\beta_1 + K_{\text{peso}})s + (1-H)(\beta_2 + K_{\text{ieso}})]}. \tag{29}$$

By selecting $K_{\text{peso}} = \omega^2$, $K_{\text{ieso}} = 2\omega$ (where $\omega = 600$), $k_p = 12$, and $b_0 = 813$, then combining Eqs. (27), (29), and (15), we can plot the Bode diagram of the compensated open-loop transfer function, as shown in Fig. 12.

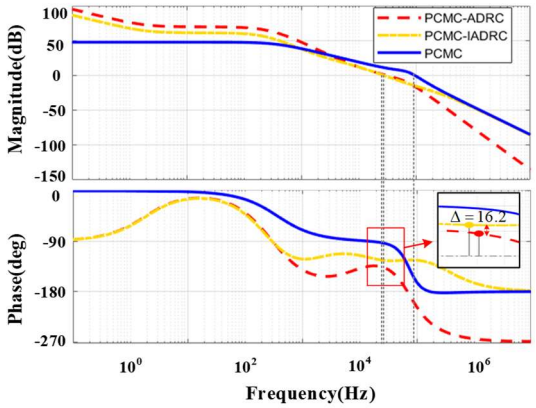

Fig. 12. The compensated open-loop Bode plot

In the figure, the solid blue line represents the Bode plot of the single PCMC strategy, the dashed red line represents the Bode plot of the PCMC-ADRC control, and the dashed orange line represents the Bode plot of the PCMC-IADRC control adapted from ADRC.

Before adding ADRC compensation, the stability margin of the system is small and the system crossing frequency is too high, which adversely affects the stability and response speed of the system. Following the incorporation of the ADRC voltage outer loop, the crossing frequency decreased to approximately 31 kHz, while the phase margin increased to 40.2°. With the improved ADRC, the crossing frequency further decreased to 29 kHz, and the phase margin increased to 56.8°. Notably, the improved system significantly enhances stability without compromising rapid response. The stability margin was effectively increased, better aligning with loop stability criteria, where the crossing frequency ideally falls between one-tenth and one-fifth of the switching frequency, and the phase margin ranges from 45° to 60°.

4.3. Current sharing strategy

In practical systems with multiple parallel branches, the impedance of the lines and the parameters of electronic components cannot be completely identical, resulting in slightly different currents flowing through each branch during actual operation. If there is an uneven distribution of current, it may lead to one branch experiencing excessive current, causing its components to age prematurely and result in severe heating due to prolonged overload, ultimately leading to the system malfunctioning.

The traditional current equalization methods mainly include droop method and active current equalization method.

The droop method is a passive current equalization technique, which is based on a drop in load voltage to increase its output current, thus equalizing the current. When the output current of a converter exceeds that of other converters, its output voltage drops slightly, which results in a voltage difference between its output voltage and that of the other converters. Based on this difference, the converter automatically adjusts its output voltage to bring its output current closer to that of the other converters, thus equalizing the current. This method is suitable for medium and small power devices. However, its effectiveness is relatively poor under light load conditions [24].

The active current equalization method mainly consists of two major categories: master-slave current equalization and independent current loop equalization.

In this paper, peak current control is used to achieve a precise current equalization effect. This is an active current equalization method differentiated from droop control. The on-time of the switching tubes is adjusted by controlling the peak value of the current to ensure that the parallel DC–DC converters contribute essentially equal currents in each switching cycle [25, 26]. The performance is especially excellent during dynamic load variations and input voltage fluctuations. Figure 13 illustrates the main logic control diagram in this paper.

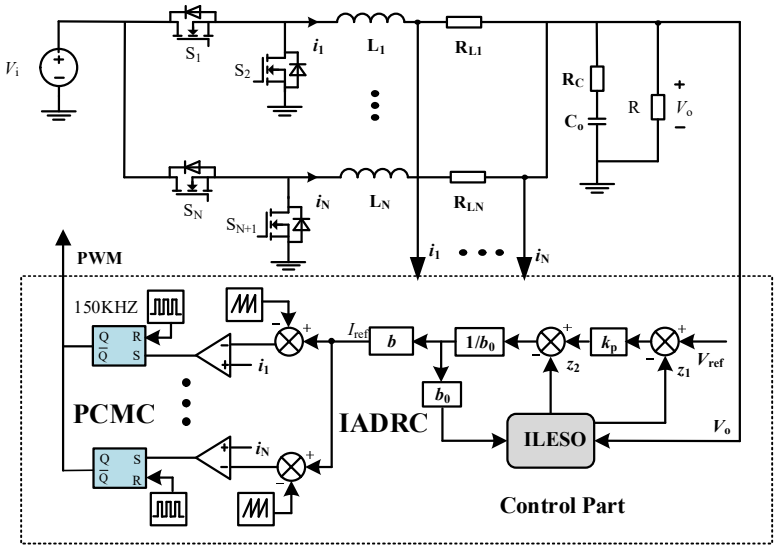

Fig. 13. The logic control diagram

5. Experiments and results analysis

The experiment was conducted using a TMS280025 as the control core, constructing a prototype with dimensions of $8\times5.7\times1.7$ cm, rated power of 1000 W, and power density of 12.9 W/cm^2. The specific parameters are provided in Table 1 above. The experimental setup is illustrated in Fig. 14.

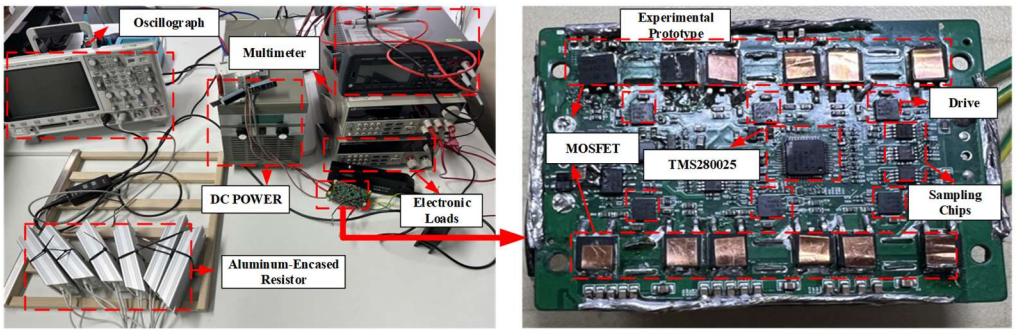

Fig. 14. Photograph of the experimental setup

5.1. Steady state performance experimental

The steady-state experiments compare four control methods: PCMC-IADRC, PCMC-ADRC, PCMC-PI, and PI dual-loop control's steady-state output voltage ripple. When the input voltage is 60 V and the output voltage is 28.5 V, the waveforms of the four algorithms are shown in Fig. 15.

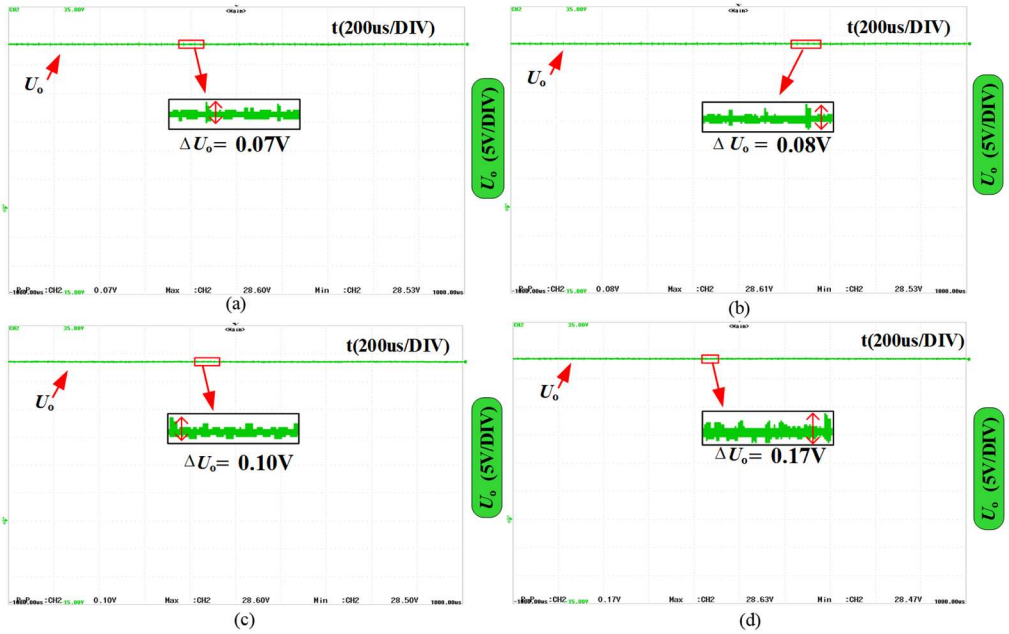

Fig. 15. Waveforms of the four algorithms at steady state output: (a) PCMC-IADRC; (b) PCMC-ADRC; (c) PCMC-PI; (d) PI dual-loop

In Fig. 15, it can be seen as follows under steady-state operating conditions, the output voltage ripple is lower with the PCMC, that is because during each switching cycle, the PCMC is able to accurately adjust the operating time of the switching tubes to match the load demand and input

voltage variations, thus minimizing output voltage fluctuations. In addition, the use of ADRC outer-loop control improves the robustness of the system, effectively eliminates interference signals from the power supply, load or environment, and further reduces output voltage fluctuations and ripples compared to ordinary PCMC. The difference in steady state performance between the improved ADRC and the normal ADRC is not significant.

5.2. Dynamic performance experimental

The dynamic experiments compared four control methods: PCMC-IADRC, PCMC-ADRC, PCMC-PI, and PI dual-loop control. The settling time, t_s was defined as the time to achieve 2% of the steady-state output value. When the input voltage U_{in} = 60 V and the output voltage U_o = 28.5 V under full load, the startup voltage waveforms for the four different control methods are shown in Fig. 16. Among them, the startup time are approximately 121 ms for PCMC-IADRC, 117 ms for PCMC-ADRC, 155 ms for PCMC-PI, and 210 ms for PI dual-loop control.

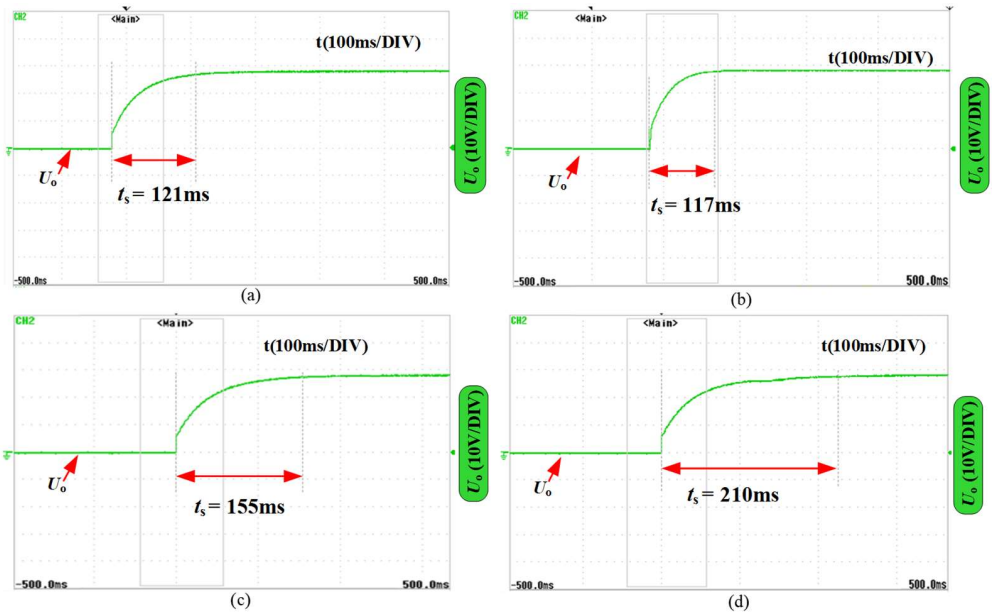

Fig. 16. Voltage startup waveforms for the four control methods: (a) PCMC-IADRC; (b) PCMC-ADRC; (c) PCMC-PI; (d) PI dual-loop

From the Fig. 16, it can be observed that PCMC-ADRC has the fastest startup time, followed by PCMC-IADRC, and is significantly better than the other two algorithms. Thus, PMCM-IADRC demonstrates good startup speed.

In the load step experiment the four methods are compared under the same conditions as before. The load transitions from half-load to full-load, and the results are shown in Fig. 17.

The output voltage regulation time for PCMC-IADRC is 25 ms with an overshoot voltage of 2.3 V; for PCMC-ADRC it is also 25 ms with an overshoot voltage of 3.3 V; for PCMC-PI it is

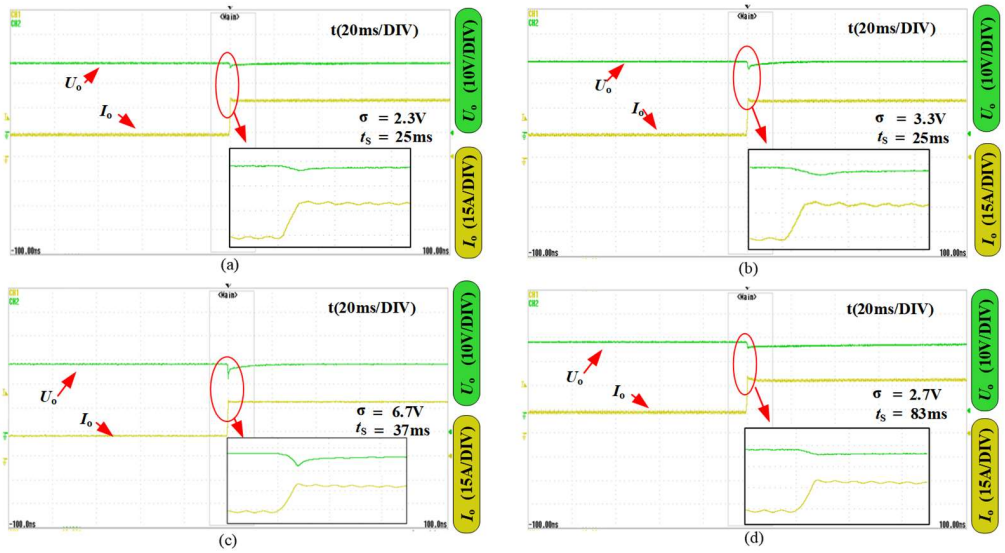

Fig. 17. The response of the four control methods to sudden change in load from half-load to full-load: (a) PCMC-IADRC; (b) PCMC-ADRC; (c) PCMC-PI; (d) PI dual-loop

32 ms with an overshoot voltage of 6.7 V; and for the PI dual-loop it is 100 ms with a voltage change of 3.7 V. From the graph, it can be seen that compared to the traditional voltage and current dual-loop control method, using peak current control can significantly improve the response speed, but the voltage change will be higher. However, the use of ADRC outer loop can suppress the voltage change. PCMC-ADRC and PCMC-IADRC have almost the same regulation time, but PCMC-IADRC has a smaller voltage change.

The experimental waveforms of the four control schemes when the load transitions from full-load to half-load are shown in Fig. 18.

It can be observed that the experimental results of transitioning from half-load to full-load are similar. Therefore, the PCMC-IADRC scheme proposed in this paper has the best resistance to sudden load changes.

Under the condition where the output power is fixed at 1000 W and other variables remain the same as described earlier, the dynamic response graphs of the four methods to a sudden change in input voltage from 40 V to 60 V are shown in Fig. 19.

Due to the limitations of the experimental power supply performance, the voltage change occurs relatively slowly, taking about 100 ms to transition from 40 V to 60 V. Under these conditions, the adjustment time for PCMC-IADRC is approximately 110 ms with almost no overshoot voltage. PCMC-ADRC has a similar adjustment time of around 110 ms with minimal overshoot voltage, about 0.5 V. PCMC-PI also has an adjustment time of around 110 ms with an overshoot voltage of about 2.5 V. In comparison, the adjustment time for PI dual-loop control is 180 ms with an overshoot of 2.1 V. While the adjustment speed of PCMC-IADRC is comparable to PCMC-ADRC and PCMC-PI, it achieves the smallest overshoot voltage among the four methods. Conversely, the dual-loop PI control exhibits the slowest adjustment speed among the tested methods.

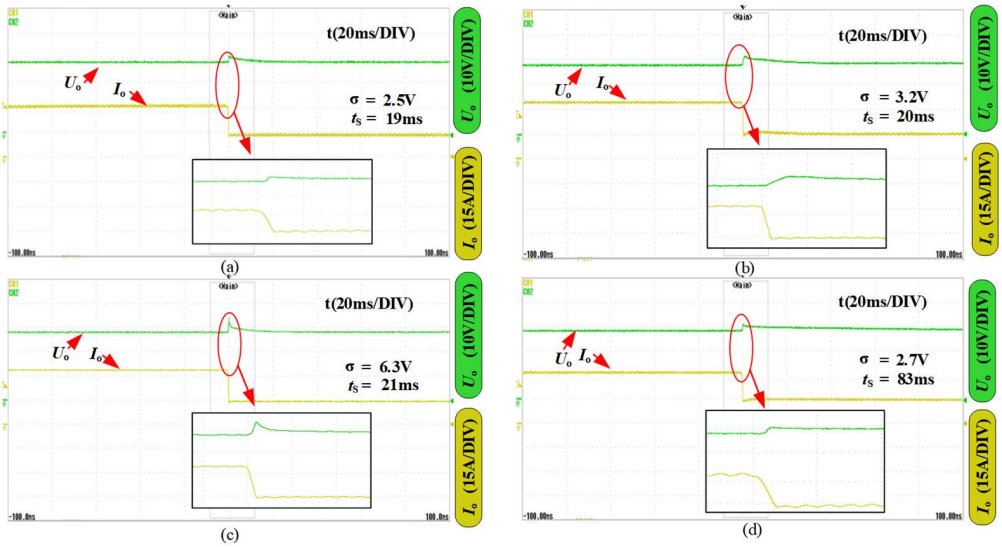

Fig. 18. The response of the four control methods to sudden change in load from full-load to half-load: (a) PCMC-IADRC; (b) PCMC-ADRC; (c) PCMC-PI.; (d) PI dual-loop

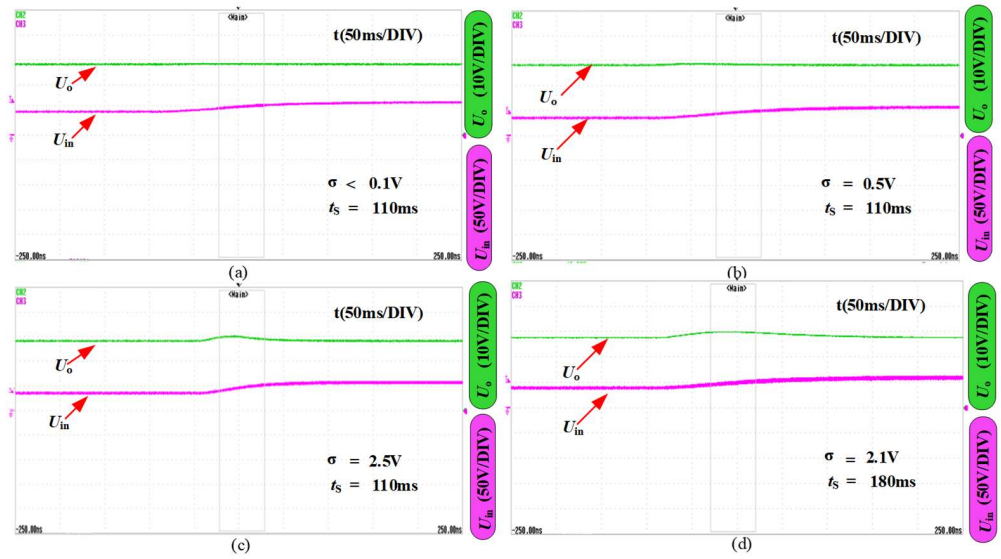

Fig. 19. The response of four control methods to a sudden change in input voltage from 40 V to 60 V: (a) PCMC-IADRC; (b) PCMC-ADRC; (c) PCMC-PI; (d) PI dual-loop

The output voltage response when the input voltage suddenly changes from 60 V to 40 V under the same conditions is shown in Fig. 20.

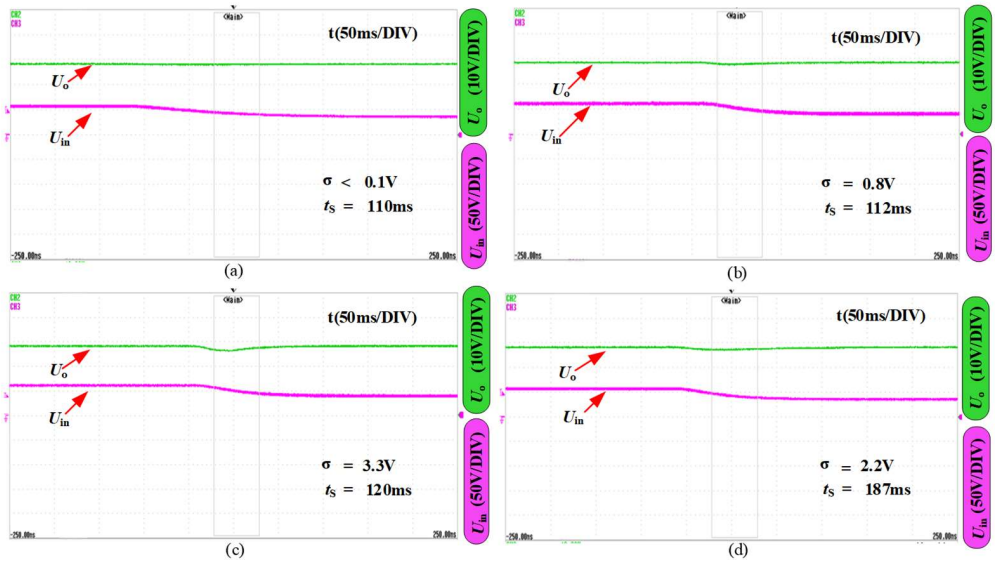

Fig. 20. The response of four control methods to a sudden change in input voltage from 40 V to 60 V: (a) PCMC-IADRC; (b) PCMC-ADRC; (c) PCMC-PI; (d) PI dual-loop

It can be seen that the PCMC-IADRC is also better able to resist perturbations in the input voltage. Demonstrates the good robustness of the control method.

5.3. Current sharing experimental

Due to limitations of the experimental setup, direct measurement of the inductor current with a current probe is not feasible. Consequently, the inductor current must be measured from the output of the current sensing chip. However, because of the limited bandwidth of the sensing chip, the measured waveform exhibits some distortion. When the input voltage is U_{in} = 60 V, output voltage is U_o = 28.5 V, and output power is 1000 W, the voltage control result without current sharing effect is shown in Fig. 21(a). The result with PCMC-IADRC current sharing is shown in Fig. 21(b). It can be observed that the PCMC-IADRC algorithm achieves good current sharing effect.

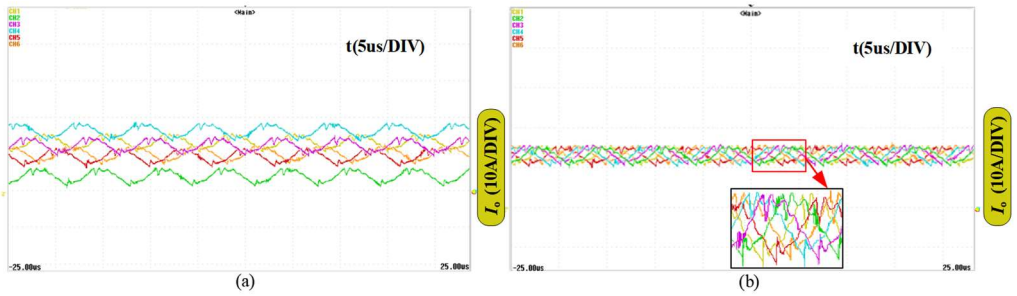

Fig. 21. The waveforms of the six inductor currents: (a) inductor current waveform without using current sharing algorithm; (b) inductor current waveform after using PCMC-IADRC current sharing algorithm

5.4. Efficiency experiment

For this experimental prototype, the losses are mainly composed of MOSFETs, inductance and drive losses. The MOSFETs losses include pass-state losses, switching losses etc. The loss calculation for MOSFTs can be obtained from Eq. (29).

$$P_{\mathrm{MOS}} = P_{\mathrm{CM}} + P_{\mathrm{swM}} = R_{\mathrm{DS}} \cdot I_{\mathrm{Drms}}^2 + U_{\mathrm{in}} \cdot f_s \cdot \left[\left(\left| \frac{I_o}{N} - \frac{I_{\mathrm{pp}}}{2} \right| \right) \cdot \frac{t_{\mathrm{on}}}{2} + \left(\frac{I_o}{N} + \frac{I_{\mathrm{pp}}}{2} \right) \cdot \frac{t_{\mathrm{off}}}{2} \right] + U_o \cdot f_s \cdot \left[\left(\left| \frac{I_o}{N} - \frac{I_{\mathrm{pp}}}{2} \right| \right) \cdot \frac{t_{\mathrm{on}}}{2} + \left(\frac{I_o}{N} + \frac{I_{\mathrm{pp}}}{2} \right) \cdot \frac{t_{\mathrm{off}}}{2} \right] + 4 \cdot V_{\mathrm{in}}^{1.5} \cdot C_{oss} \cdot \sqrt{V}_{\mathrm{DS}} \cdot \frac{f_{\mathrm{sw}}}{3}, \quad (30)$$

where P_{CM} denotes the turn-on state loss, P_{swM} denotes the turn-on and turn-off loss, R_{DS} denotes the drain-source turn-on resistance, I_{Drms} denotes the root-mean-square value of the turn-on state current, and ton and toff denote the rise time of the current when the MOSFETs turn on and the fall time of the voltage when they are turned off. U_o, U_{in}, and I_o denote the output voltage, the input voltage, and the output current, respectively. I_{pp} denotes the peak-to-peak value of inductor current and f_{sw} denotes the switching frequency [27]. N represents the number of branches in parallel. Inductor losses are mainly core losses, copper losses and winding dielectric losses. Inductor losses are mainly core losses, copper losses and winding dielectric losses. Inductive loss calculation can be expressed as Eq. (30).

$$\begin{cases} P_{\mathrm{v}} = C_M \cdot f_{\mathrm{sw}}^{\alpha} \cdot B^{\beta} \\ P_{\mathrm{COP}} = I_L^2 \cdot R_L \\ P_{\mathrm{cd}} = d\omega^3 L^2 C_d \end{cases}, \quad (31)$$

where P_{v}, P_{cop}, and P_{cd} denote the iron loss, copper loss, and winding dielectric loss of the inductor, respectively. cm, α, and β are the parameters for the core loss calculation and B is the flux density. The final drive loss can be calculated from Eq. 32.

$$P_{Qd} = U_{\mathrm{gs}} \cdot Q_g \cdot f_{\mathrm{sw}}, \quad (32)$$

where U_{gs} denotes the gate source voltage and Q_g denotes the gate charge total. Substituting all the parameters of the experimental prototype into the above equation gives the percentage of loss per category at rated power can be obtained as shown in Fig. 22.

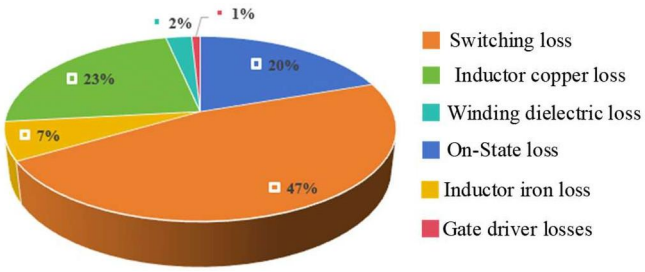

Fig. 22. Percentage loss of each part of the experimental prototype

The final calculated theoretical loss is 38.11 W and theoretical efficiency is 96.29%.

When the input voltage U_{in} = 60 V and the output voltage U_o is 28.5 V, it can be seen from Fig. 23 that the efficiency is approximately 94.5% at 200 W. As the power increases, the efficiency gradually increases, reaching the highest efficiency of 96.9% at around 700 W. However, as the power continues to increase, the efficiency decreases, reaching 95.8%at the rated 1000 W, general agreement with theoretical calculations.

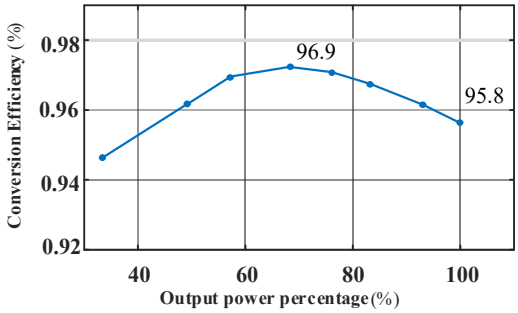

Fig. 23. Efficiency graph at different power

6. Conclusions

In this paper, a PCMC-IADRC control algorithm is proposed for a six-phase isochronous buck converter applied to UAVs. By combining the peak current control with the improved ADRC control, the response speed and disturbance rejection capability of the system are significantly enhanced. Finally, experimental comparisons were conducted with conventional ADRC outer loop control, traditional peak current dual closed-loop control, and average voltage-current dual closed-loop control. The experimental results demonstrate that the proposed improved active disturbance rejection control combined with peak current control for the six-phase interleaved parallel synchronous buck converter offers:

1. Excellent dynamic response capability. Compared with the other three control methods, it exhibits superior start-up speed and optimal regulation speed, and can quickly recover the set output voltage when disturbed. In addition, it has the smallest output voltage fluctuation under disturbances among the four control methods.
2. Achieves good current sharing. With the current sharing algorithm, the amplitude of each inductor current becomes identical, which is beneficial for the long-term operation of the system.
3. High efficiency and high-power density. The experimental prototype is compact, achieving a power density of 12.9 W/cm^3. With an input voltage of 60 V, output voltage of 28.5 V, and rated power of 1000 W, the maximum efficiency reaches 96.9%, while the rated efficiency can reach 95.8%.

Acknowledgements

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