

# Properties of the power conditioning system with a five-level cascaded converter and supercapacitor energy storage

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**Abstract.** The paper presents the power conditioning system (PCS) with a five-level cascaded H-bridge converter and supercapacitor energy storage. The paper focuses on such properties of a power electronic converter as its operation, power losses, start-up as well as the DC-link voltage balancing method and controller. A laboratory model of the PCS and its test results have been presented.

**Key words:** cascaded H-bridge multilevel converters; power conditioning system, power quality.

## 1. Introduction

The enhancement of reliability of electric power networks demands innovative technologies. One of them is the concept of smart grids the main goal of which is to improve electrical energy delivery to loads connected to those grids. Such improvement can be performed in many ways i.e. by using flexible alternating current transmission controllers (FACTS), energy storage systems, distribution generation, etc [1]. Similarly to conventional power systems, smart grids can also be vulnerable to power quality problems. There are many solutions which can eliminate such power quality problems [1]: active power filters, unified power quality conditioning systems. The power conditioning system (PCS) presented in the paper is considered the most comprehensive means for improving power quality. It is usually achieved by reactive power and current harmonics compensation, limiting the currents of pulsating loads and ensuring an uninterrupted power supply for sensitive loads. It means that the power conditioning system has to consist of a power electronic converter, an energy storage and a control circuitry. Depending on the voltage level of the grid, a power electronic converter must have different topologies. In a medium voltage grid it is typical to use multilevel converters [2, 3]. The fast reaction to rapid changes of the grid voltage or load current is the matter of great importance in the PCS. This feature can be achieved only with the new types of energy storages, like: flywheels, supercapacitors or superconducting magnetic coils. In this paper the power conditioning system with supercapacitor energy storage is described. Supercapacitors were chosen because of their reasonable cost [4, 5].

Multilevel converters are divided into three basic topologies i.e. diode-clamped, flying capacitor and cascaded converters. Each of  $n$ -level basic converter topology requires  $2(n - 1)$  active switches per phase. The number of diodes in the diode-clamped converter increases dramatically with the voltage level  $n$  [6]. Due to this problem and DC-link volt-

age balancing issues, diode-clamped converters are seldom used in industrial applications [2]. Similarly, flying capacitor converters consist of a large number of capacitors, which increase the complexity of the converter performance. Among these three converter topologies the cascaded converter has the smallest number of power part components and, due to its modularity, is often used in medium voltage applications [2]. One of the disadvantages of the cascaded converter is that it demands the use of  $3(n - 1)/2$  separate DC voltage sources, which is typically performed by using a multi-winding transformer. This is not necessarily applicable when the energy storage is based on supercapacitors.

The authors have chosen a five-level cascaded H-bridge converter which consists of six separate supercapacitor modules. The power part of the power conditioning system has been presented in Fig. 1. One of the power electronic cells that are present in each phase is depicted in Fig. 2. In the paper the operation of the cascaded H-bridge converter has been described. The PCS can operate in different modes, in which different power quality parameters are enhanced. These modes depend on the grid voltage and the load current levels. Generally, the PCS produces three-phase currents which together with the load currents contribute to the sinusoidal grid currents. This operation is performed by the generation of certain converter output voltages.

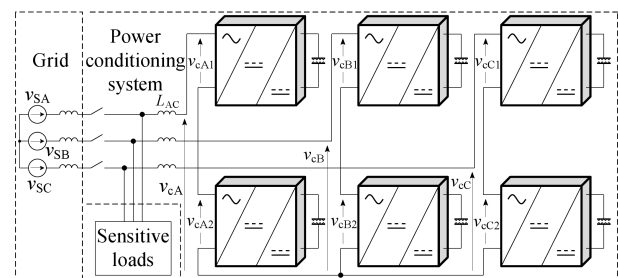


Fig. 1. The power conditioning system with a five-level cascaded H-bridge (CHB) converter and supercapacitor energy storage

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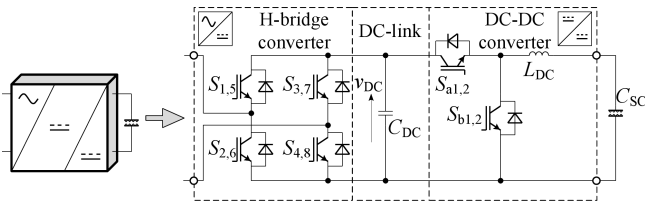


Fig. 2. One cell of the PCS consisting of an H-bridge converter, a DC-link capacitor and a DC-DC converter

The paper first focuses on the conditions that must be fulfilled to generate the demanded output voltage. Basing on the achieved results, the calculations of power losses that are generated in the PCS with a five-level CHB converter have been presented.

One of the most important issues related to multilevel converters is the DC-link voltage balancing. This problem together with a description of the PCS control circuit is briefly presented in the paper.

A laboratory model of the PCS with a five-level CHB converter and supercapacitor energy storage was assembled and its proper operation was proved experimentally during the start-up and grid voltage dip.

## 2. Cascaded H-bridge converter

Each phase of a five-level cascaded H-bridge converter consists of two H-bridge converters connected in series, as presented in Fig. 1. The output phase voltage of the converter is the sum of the output voltages of constituent H-bridges, e.g.  $v_{cA} = v_{A1} + v_{A2}$ . One of typical modulation strategies for generating the output voltage in a CHB converter is the Phase Shifted Pulse Width Modulation method (PS-PWM) [6, 7]. The Authors have chosen the PS-PWM due to the ease of implementing the DC-link voltage balancing method into the microprocessor based controller [8]. The PS-PWM strategy is based on a comparison of modulating signal  $S_M$ , and triangular carriers  $S_N$  (in a five-level converter there are 4 carriers  $S_{N1}-S_{N4}$  phase-shifted by  $\pi/2$ ). The carriers  $S_{N1}$  and  $S_{N3}$  are related to the switches  $S_1, S_2, S_3$  and  $S_4$  of the upper H-bridge converter and the carriers  $S_{N2}$  and  $S_{N4}$  are related to the switches  $S_5, S_6, S_7$  and  $S_8$  of the bottom H-bridge converter which has been presented in Fig. 3.

A large number of carrier signals is a drawback of this modulation strategy. A reduction of the number of carrier signals using the limited number of PWM outputs in a control system is described in [7].

It can be seen from Fig. 3 that signals  $s_2, s_3, s_6$  and  $s_7$  are not depicted. This is due to the fact that these signals are complementary to  $s_1, s_4, s_5$  and  $s_8$  respectively. For other phases the principles are the same with the exception of the phase shift of  $2\pi/3$  between modulating signals  $S_{MA}, S_{MB}$  and  $S_{MC}$ .

It is important to note that PWM methods are characterised by typical coefficients such as the amplitude modulation index  $m_a$  and frequency index  $m_f$ , given by

$$m_a = \frac{A_M}{A_N}, \quad (1)$$

$$m_f = \frac{f_N}{f_M} \quad (2)$$

where  $A_M, f_M$  and  $A_N, f_N$  are the peak values and frequencies of the modulating signal  $S_M$  and carriers  $S_N$  respectively.

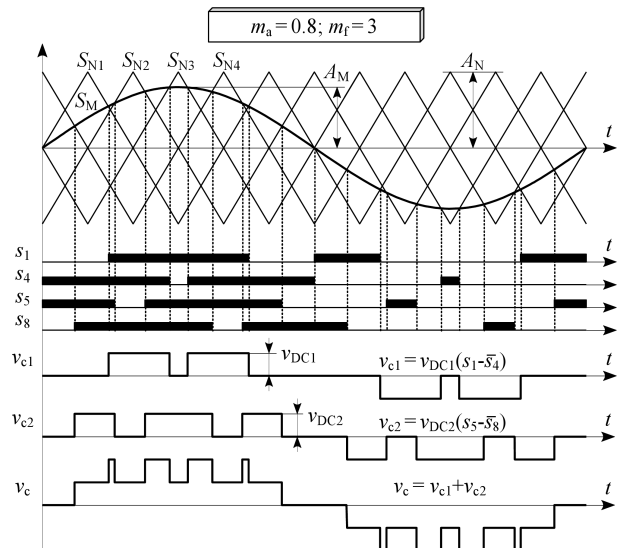


Fig. 3. Switching states and output voltage  $v_c$  of one phase of the five-level cascaded H-bridge converter

From the modulation theory it is well known that for frequency indices  $m_f > 20$  the average output voltages  $\langle v_{c1} \rangle_{T_N}$ ,  $\langle v_{c2} \rangle_{T_N}$  (averaged over the switching period  $T_N = 1/f_N$ ) are proportional to the modulating signal  $S_M = m_a \sin(\omega_M t)$  [9], which can be written by (3).

$$\langle v_{c1} \rangle_{T_N} = S_{M1} v_{DC1} = m_a \sin(\omega_M t) v_{DC1}, \quad (3a)$$

$$\langle v_{c2} \rangle_{T_N} = S_{M2} v_{DC2} = m_a \sin(\omega_M t) v_{DC2}, \quad (3b)$$

$$\langle v_c \rangle_{T_N} = m_a \sin(\omega_M t) (v_{DC1} + v_{DC2}), \quad (3c)$$

where  $\omega_M$  is the angular frequency of the modulation signal  $S_{M1}$  (for an upper H-bridge converter) and  $S_{M2}$  (for a lower H-bridge converter). The Eqs. (3) are valid for the case when modulating signals  $S_{M1}, S_{M2}$  are equal, which is normally fulfilled. As will be shown later, the modulating signals  $S_{M1}$  and  $S_{M2}$  can be different if the DC-link voltage balancing method is used. For the sake of simplicity of power losses analyses, it is assumed that  $S_{M1} = S_{M2}$  for each phase of the converter.

## 3. Operation of the power conditioning system connected to the grid

The operation of the PCS can be explained by using a simple one-phase model [1] of a system represented by the grid voltage source  $V_S$ , the lossless line inductor  $L_{AC}$  and the PCS voltage source  $V_c$  connected in series (Fig. 4a). In this analysis all voltages and currents are assumed to be sinusoidal and the load is not connected.

In Fig. 4b the vector diagram of three voltages  $\underline{V}_S, \underline{V}_L$  and  $\underline{V}_c$  is presented. It has been assumed that all vectors are analysed in a rotating reference frame oriented along the grid

voltage vector  $\underline{V}_S$ . The PCS can generate current  $\underline{I}_c$  (perpendicular to the vector  $\underline{V}_L$ ), which is phase-shifted to  $\underline{V}_S$  by the angle  $\psi$ . When the angle  $\psi$  varies from 0 to  $2\pi$ , the end of the PCS voltage vector  $\underline{V}_c$  rotates around the end of the vector  $\underline{V}_S$  (circles with their centre located at the end of  $\underline{V}_S$ ). The maximum length of the vector  $\underline{V}_L$ ,  $V_{L\max}$  depends on the maximum length of the PCS voltage vector  $V_{c\max}$  and the grid voltage  $V_S$ , which can be written as (4).

$$V_{L\max} = V_{c\max} - V_S. \quad (4)$$

From Eq. (4) it can be seen that  $V_{c\max}$  has to be always greater than the amplitude of the grid voltage  $V_S$ . This can be written as  $V_{c\max} = \delta V_S$ , where  $\delta$  is a boost factor, typically  $\delta = 1.2-1.3$ . Because  $\delta$  is greater than 1, the power electronic converter, which is a voltage-source converter (VSC), should have a DC-link voltage higher than the amplitude of the line-to-line grid voltage. A lower boost factor  $\delta$  results in lower voltages of the line inductor, and hence lower currents. For greater  $\delta$ , currents can be higher but at a cost of higher DC-link capacitor voltage.

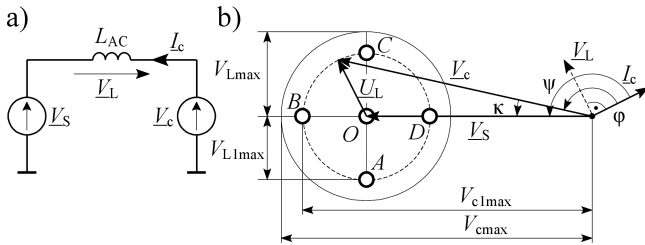


Fig. 4. The PCS connection to the grid: a) a one-phase model, b) a vector diagram presenting voltage vectors  $\underline{V}_c$ ,  $\underline{V}_L$  and  $\underline{V}_S$

Because the PCS has to generate current harmonics, the maximum voltage  $V_{L\max}$  is greater than the maximum fundamental component of the inductor voltage  $V_{L1\max}$ . Each current harmonic component demands additional voltage (with the same harmonic order) that is generated by the PCS voltage  $V_c$ . It is assumed that the PCS should generate harmonics the amplitudes of which decrease with their order of  $1/h$ , for instance as in a six-pulse diode rectifier with DC current at the output. The reactance of the line inductor for harmonics is given as (5).

$$X_{LAC h} = h\omega L_{AC}, \quad (5)$$

where  $\omega$  is the angular frequency of the line voltage  $v_s$ . Assuming the six-pulse diode rectifier is a nonlinear load, one can see from (5) that each current harmonic component demands the harmonic component of voltage  $v_c$  with nearly the same amplitude. Hence, the maximum inductor voltage for fundamental component  $V_{L1\max}$  is always lower than  $V_{L\max} = (\delta - 1)V_S$ . In the paper it is assumed that the PCS allows the generation of current harmonics of the following orders  $h = 5, 7, 11$  and  $13$ . As each harmonic component for the assumed six-pulse rectifier is generated by the inductor voltage of the same amplitude  $V_{Lh}$ , the maximum inductor voltage for the fundamental component will be one fifth of  $V_{L\max}$ ,  $V_{L1\max} \approx 0.2V_{L\max}$ . It should be noted that the afore-

mentioned limitation is only for prototyping purposes and can be different for other assumptions.

Currents can also be increased by decreasing  $L_{AC}$ , but at a cost of higher current ripples.

It should be noted that the highest PCS voltage  $V_{c\max}$  is generated for the maximum amplitude modulation index  $m_{a\max}$ , which, with third harmonic injection, is equal to  $m_{a\max} = 2/\sqrt{3} \approx 1.15$ . Knowing that for  $V_c = V_S$ , the modulation index  $m_a = (1/\delta)m_{a\max}$  and  $k_1 = I_{c1}/I_{c1\max}$ , where  $I_{c1}$  is the actual current amplitude of fundamental component,  $I_{c1\max}$  is the maximum possible amplitude of the current fundamental component,  $I_{c1\max} = V_{L\max}/X_{LAC1}$ . Using the law of cosines, modulation index  $m_a$  and the angle  $\kappa$  between the voltage vectors  $\underline{V}_c$  and  $\underline{V}_S$  can be determined.

$$m_a = m_{a\max} \left[ \left( \frac{1}{\delta} \right)^2 + \left( k_1 \left( \frac{\delta - 1}{\delta} \right) \right)^2 - 2 \frac{1}{\delta} k_1 \frac{\delta - 1}{\delta} \cos \left( \frac{3\pi}{2} - \psi \right) \right]^{1/2}, \quad (6)$$

$$\kappa = \text{sgn}(-\cos\psi) a \cos \left( \frac{\left( \frac{m_a}{m_{a\max}} \right)^2 + \left( \frac{1}{\delta} \right)^2 - \left( \frac{k_1\delta - k_1}{\delta} \right)^2}{2 \frac{m_a}{m_{a\max}} \frac{1}{\delta}} \right). \quad (7)$$

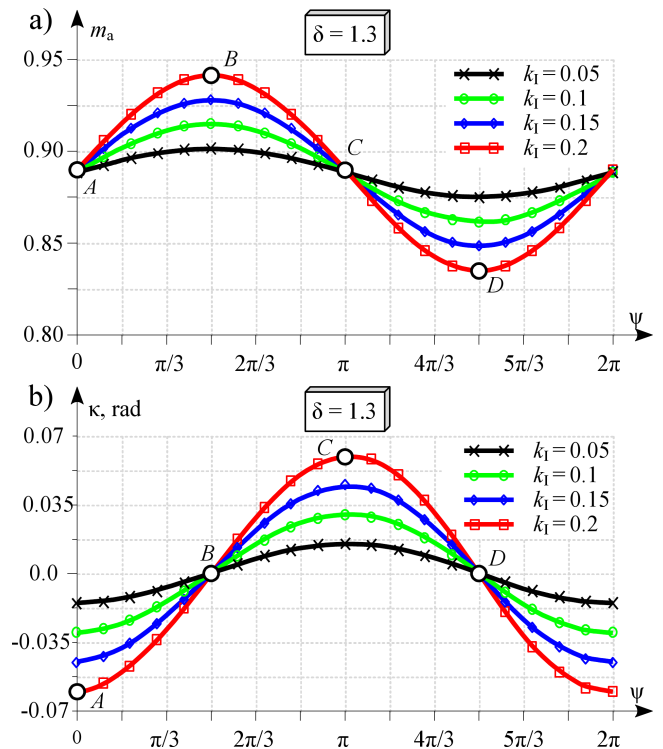


Fig. 5. The operation of the PCS: a) the modulation index  $m_a$ , b) the angle  $\kappa$  - points A-D are the same as in Fig. 4

The parameters  $m_a$  and  $\kappa$  calculated from Eq. (6) and (7) are shown in Fig. 5 as functions of the angle  $\psi$  for  $\delta = 1.3$ . This figure shows that during operation  $m_a$  and  $\kappa$  are changing in a very narrow range  $m_a = 0.83 \dots 0.94$  and  $\kappa = -0.060 \dots 0.060$ . The greatest changes occur for the

greatest values of coefficient  $k_1$ , which in this case is  $k_1 = 0.2$ . The obtained results of this analysis can be useful for the power losses analysis performed in the next section.

#### 4. Power losses in the PCS

Power losses in the PCS result mainly from the conduction and switching of semiconductor devices (IGBTs) of all the converters. The operation of the AC-DC converter has been explained in the previous section and here, basing on this analysis, the power losses calculations are presented. AC-DC converter losses and DC-DC converter losses calculated by the same method have been presented briefly below.

**Power losses of the AC-DC converter.** The conduction losses  $P_{CON}$  in the CHB converter are divided into losses in transistors  $P_{TCON}$  and diodes  $P_{DCON}$ . These losses can be calculated in the same manner as in classical two-level single-leg converter switching under the PWM method, taking into account the different number of switches. Conduction losses for a two-level single-leg converter are computed in the handbook [10] for the sinusoidal modulating signal  $S_M = m_a \sin(\omega t)$  and the sinusoidal output current  $i_c$ . In [8] this analysis is performed for the modulating signal  $S_M$  with third harmonic injection; the results of this analysis are given in (8).

$$P_{TCON} = 24 \left[ \frac{1}{2} I_{cm} V_{T0} \left( \frac{1}{\pi} + \frac{m_a}{4} \cos(\phi) \right) + I_{cm}^2 r_T \left( \frac{1}{8} + \frac{m_a}{3\pi} \cos(\phi) - \frac{m_a}{90\pi} \cos(3\phi) \right) \right], \quad (8)$$

$$P_{DCON} = 24 \left[ \frac{1}{2} I_{cm} V_{D0} \left( \frac{1}{\pi} - \frac{m_a}{4} \cos(\phi) \right) + I_{cm}^2 r_D \left( \frac{1}{8} - \frac{m_a}{3\pi} \cos(\phi) + \frac{m_a}{90\pi} \cos(3\phi) \right) \right],$$

where  $V_{T0}$ ,  $V_{D0}$  are the threshold voltages of transistor and diode respectively for conduction mode,  $r_T$ ,  $r_D$  are dynamic resistances,  $I_{cm}$  is the current amplitude of  $i_c$  and  $\phi$  is the angle between fundamental component of the voltage  $v_c$  and the current  $i_c$ ,  $\phi = \psi - \kappa$ , the number 24 comes from the number of switches that the five-level cascaded converter consists of.

Using equations (8) it is possible to calculate the conduction losses  $P_{CON} = P_{TCON} + P_{DCON}$  of the five-level cascaded converter operating in the PCS as a function of the angle  $\psi$ , when the PCS operates as a reactive power compensator (line in Fig. 4 between points B and D) or when it transfers active power from the grid to the PCS and inversely (line in Fig. 4 from point C to A). The results are presented in Fig. 6.

For this analysis it is assumed that the maximum amplitude of the current fundamental component  $I_{c1\max} = 20.4$  A, which gives the rated active power of  $P = 10$  kW; for the grid voltage  $V_{SII} = 400$  V, the line inductances are  $L_{AC} = 4$  mH and the DC-link voltages are  $V_{DC} = 190$  V, which gives

$\delta = 4v_{DC}/(\sqrt{2}V_{SII}) = 1.34$ . It is also assumed that the AC-DC converter consists of 12 IGBT modules SKM75GB063D ( $I_T = 75$  A,  $V_T = 600$  V,  $V_{T0} = 1.17$  V,  $V_{D0} = 0.92$  V and  $r_T = 16$  m $\Omega$ ,  $r_D = 7.8$  m $\Omega$  [11]). For such parameters the maximum ratio of the amplitude of the current fundamental component and the maximum current is  $k_{1\max} = 0.23$ .

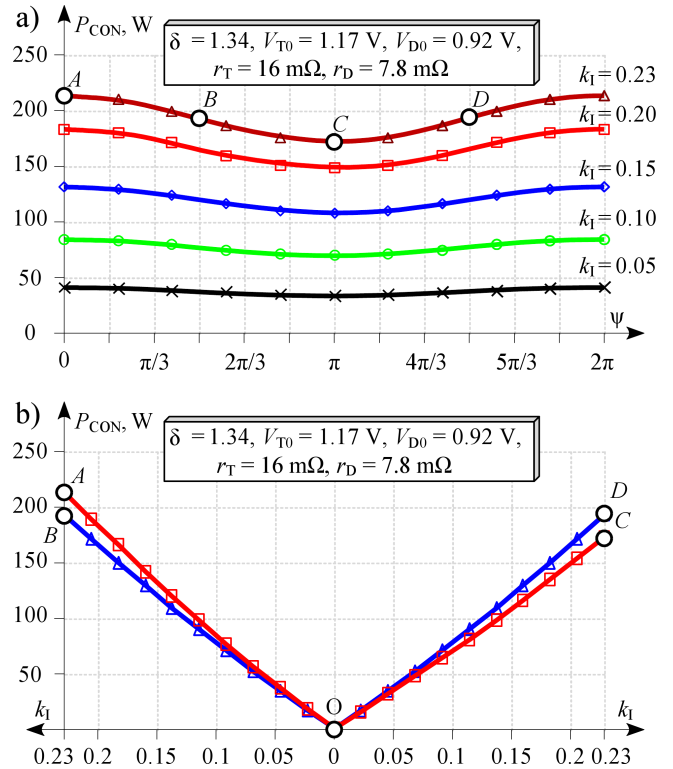


Fig. 6. The conduction power losses  $P_{CON}$  of the five-level CHB converter operating in the PCS: a)  $P_{CON}$  as a function of the angle  $\psi$ , b) for the PCS operating as a reactive power compensator (line from B to D) and taking (O-C,  $\psi = \pi$ ) or delivering (O-A,  $\psi = 0$ ) only active power from/to the grid

It should be noted that conduction power losses  $P_{CON}$  have the greatest value when the PCS delivers only active power to the grid (point A). This is because at this operating point transistors conduct for a longer time and in the applied IGBT module the transistor output characteristics are worse than in the diode one.

The maximum value of the conduction losses in the presented five-level converter is approximately equal to 215 W, which accounts for 2.2% of the rated power  $P$ .

The switching power losses  $P_{SW}$ , which occur mainly in transistors, depend on the energies of a single turn-on or turn-off process. These energies are the function of the current amplitude  $I_{cm}$  and can be expressed by (9), [8, 10, 12].

$$E_{on}(i_T) = (A_{on}i_T^2 + B_{on}i_T), \quad (9)$$

$$E_{off}(i_T) = (A_{off}i_T^2 + B_{off}i_T),$$

where for SKM75GB063 module:  $A_{on} = 59.4$  nJ/A<sup>2</sup>,  $A_{off} = -65.1$  nJ/A<sup>2</sup>,  $B_{on} = 34$   $\mu$ J/A,  $B_{off} = 37$   $\mu$ J/A [11]. For calculation of the switching losses  $P_{SW}$ , the energies  $E_{on}$  and



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$E_{\text{off}}$  are integrated over the period of fundamental frequency  $f_M$  and the result is presented in Eq. (10) and Fig. 7.

$$P_{\text{SW}} = 24f_N I_{\text{cm}} \left( I_{\text{cm}} \frac{A_{\text{on}} + A_{\text{off}}}{4} + \frac{B_{\text{on}} + B_{\text{off}}}{\pi} \right) \frac{V_{\text{DC}}}{V_T}. \quad (10)$$

In the five-level CHB converter each of 24 transistors conducts the same current, so the switching power loss in each transistor is the same (it corresponds to the number 24 in Eq. (10)). The switching power losses  $P_{\text{SW}}$  are the function of current amplitude  $I_{\text{cm}}$  and depend linearly on the switching frequency  $f_N$  and on the blocking voltage, which is equal to  $V_{\text{DC}}$ .  $V_T = 300$  V is the blocking voltage for which coefficients  $A$  and  $B$  were measured by the IGBT manufacturer.

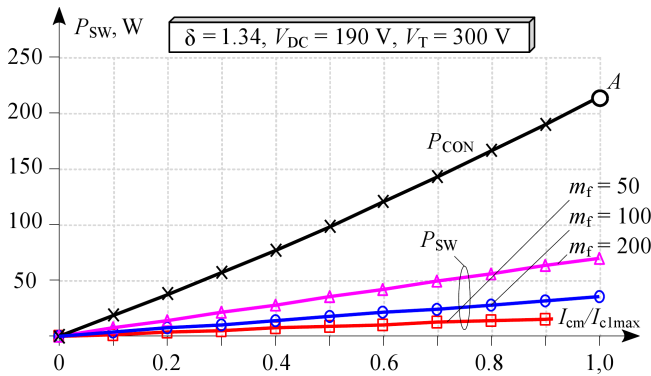


Fig. 7. The switching power losses  $P_{\text{SW}}$  of the five-level CHB converter operating with the sinusoidal output current  $i_c$  for different frequency indices  $m_f$  compared to the conduction power losses  $P_{\text{CON}}$  (O-A,  $\psi = 0$ )

From Fig. 7 it can be seen that the switching power losses  $P_{\text{SW}}$  compared to the conduction power losses  $P_{\text{CON}}$  are considerably small, even for frequency indices  $m_f > 100$  ( $f_N > 5$  kHz). Other power losses like losses due to diode reverse recovery, in DC-link capacitors, in copper wires are smaller than losses in CHB converter and line inductors, so they are not investigated here thoroughly although they can account for up to 5–10% of the total power losses.

The line inductor power losses significantly contribute to power losses in the PCS. These losses exist in copper winding and in the ferromagnetic core. The equivalent line inductor resistance, which can represent power losses in the inductor, is not constant due to nonlinear properties of hysteresis and eddy currents in the core. Regardless of the complex nature of the power losses in the line inductor, these power losses can be estimated using the quality factor  $Q = \omega L_{\text{AC}}/R_L$ , which for typical industrial line inductor is equal to  $Q = 6-15$  at the fundamental frequency. Assuming the quality factor and inductance of the analysed case  $L_{\text{AC}} = 4$  mH, the equivalent inductor resistance (at the fundamental frequency) is  $R_L = 85-210$  m $\Omega$ . Power losses in such line inductors in three phases for the rated current  $I_{c1\text{max}} = 20.4$  A are equal to  $P_{\text{LAC}} = 52-131$  W. Power losses in the line inductors are also generated due to current ripples, but they are significantly small, especially when multilevel converters are used [13].

In Fig. 8 one can see a comparison of calculated total

power losses  $P_{\text{PCSC}}$  with the measured power losses  $P_{\text{PCSM}}$  in the PCS later presented in this paper. Both power losses are obtained in reactive power compensation mode; consequently, they only embrace power losses in the CHB converter  $P_C$  and line inductors  $P_{\text{LAC}}$  plus extra losses in wires. The maximum calculated total power losses of the PCS (for  $I_{\text{cm}} = I_{c1\text{max}}$ , frequency index  $m_f = 50$ ) are equal to  $P_{\text{PCSC}} \approx 325$  W, which accounts for 3.3% of rated power  $P$ . In point A the PCS can have higher power losses equal to  $P_{\text{PCSCmax}} \approx 345$  W.

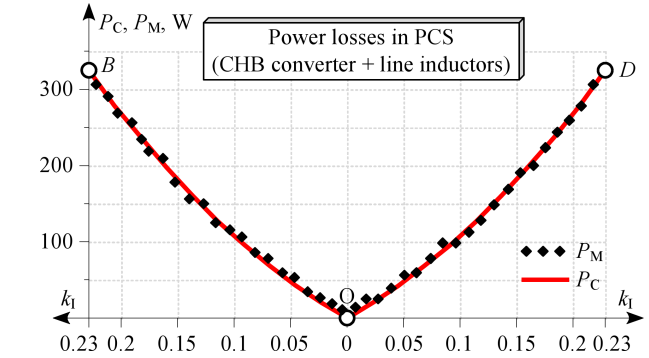


Fig. 8. A comparison of calculated and measured PCS power losses  $P_{\text{PCSC}}$  and  $P_{\text{PCSM}}$

The calculated power losses  $P_{\text{PCSC}}$  presented in Fig. 8 include the conduction and switching power losses in CHB converter, power losses existing in CHB converter due to diode reverse recovery [8] and power losses in DC-link capacitors due to equivalent series resistance  $R_{\text{CESR}}$ . Power losses in six DC-link capacitors, calculated using (11), are based on the capacitor current of 100 Hz that has an amplitude of  $1/2 I_{\text{cm}} m_a$  [8].

$$P_{\text{CAP}} = \frac{6}{8} I_{\text{cm}}^2 m_a^2 R_{\text{CESR}}, \quad (11)$$

where in the analysis  $R_{\text{CESR}} = 62$  m $\Omega$ .

Power losses in the line inductor were measured separately. The results of measured  $P_{\text{LACM}}$  and calculated power losses  $P_{\text{LACC}}$  are presented in Fig. 9. For calculations it was assumed that quality factor  $Q = 8.8$ .

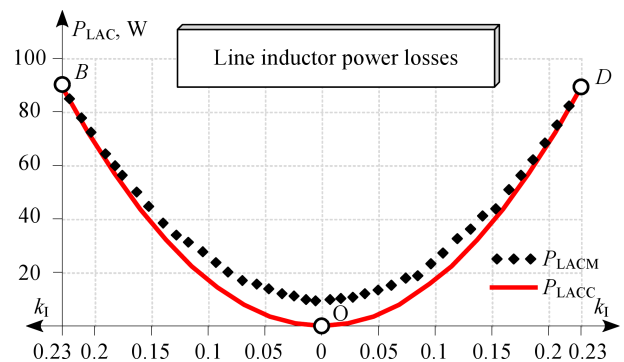


Fig. 9. A comparison of calculated and measured power losses  $P_{\text{LACC}}$  and  $P_{\text{LACM}}$  in line inductors in three phases

Figure 9 shows the difference between the measured and calculated line inductor power losses. This difference with

the current reaching  $I_c = 0$  ( $k_I = 0$ ) results from the losses generated by high frequency ripple currents and equals approximately 10 W. As was mentioned before, the power losses  $P_{LACC}$  are calculated from the assumed quality factor  $Q = 8.8$  with the current  $I_{cm} = I_{c1max}$ ; thus  $P_{LACC} = P_{LACM}$  in this case.

**Power losses of the DC-DC converter.** The bidirectional DC-DC converter operates as a synchronous step-down (for charging of the supercapacitors) or step-up converter (for discharging of the supercapacitors). The highest power losses occur in this converter when the supercapacitors current is at its limit i.e. when the supercapacitors are almost discharged. In the analysed PCS, the limit value of the supercapacitor current is equal to  $I_{SCmax} = 30$  A.

The PCS has the rated power  $P = 10$  kW, DC-link voltages  $V_{DC} = 190$  V, and the maximum voltage across the supercapacitor tank is equal to  $V_{SCmax} = 120$  V. For the rated power of  $P/6$ , because there are six similar DC-DC converters, the voltage across the supercapacitor at which the maximum current occurs is equal to  $V_{SCP} = P/(6I_{SCmax}) = 55.5$  V, below this voltage the PCS can no longer charge or discharge a supercapacitor at the rated power  $P$ .

Power losses in the DC-DC converters exist mainly due to the conduction and switching losses in transistors. It is assumed that the supercapacitor current is equal to  $I_{SCmax}$ . The conduction losses for both transistors of six DC-DC converters are equal to (12).

$$\begin{aligned}
 P_{CON} &= 6(P_{CONh} + P_{CONl}) = \\
 &= 6v_T I_{SCmax} (D + (1 - D)) = \\
 &= 6(V_{T0} + I_{SCmax} r_T) I_{SCmax} = \\
 &= 6(V_{T0} I_{SCmax} + I_{SCmax}^2 r_T),
 \end{aligned} \tag{12}$$

where  $P_{CONh}$  and  $P_{CONl}$  are the conduction power losses of high and low-side transistors,  $D$  is a duty cycle,  $V_{T0}$  and  $r_T$  are the parameters of the output characteristics of the transistors, here the same as the ones used in the AC-DC converter. It can be seen that in this converter the duty cycle  $D$  does not influence the power losses. The conduction losses  $P_{CON}$  are equal to approx. 300 W (for SKM75GB063), which accounts for 3% of the power  $P$ . It should be mentioned here that the power losses in the DC-DC converter exist only when there is a transfer of energy between the supercapacitors and the grid.

Switching power losses occur only in one transistor, in the high-side transistor for the step-down converter operation and in the low-side transistor for the step-up operation [14]. The switching power losses  $P_{SW}$  can be evaluated from (13).

$$P_{SW} = 6f_{NDC} I_{SCmax} V_{DC} \frac{t_{on} + t_{off}}{2}, \tag{13}$$

where  $f_{NDC}$  is the switching frequency equal to 15 kHz,  $t_{on}$  and  $t_{off}$  are the switching times during the turn-on and turn-off of the transistor, which are given in datasheet [11],  $t_{on} = 110$  ns,  $t_{off} = 400$  ns. The switching losses  $P_{SW}$  of all six DC-DC converters are equal to 90 W, which accounts for 0.9% of the rated power  $P$ .

Other sources of power losses are inductors  $L_{DC}$ , which are made of the iron powder core –26 in T650 size (outer dimension equal to 6.5 inches – 165.1 mm) with 65 turns of 10 mm<sup>2</sup> tin plated copper wire. These inductors for current  $I_{SCmax}$  have the inductance  $L_{DC} = 770$   $\mu$ H and power losses  $P_{LDC}$  at the frequency  $f_{NDC} = 15$  kHz are equal to  $P_{LDC1/6} = 40$  W in each of the inductors. This gives  $P_{LDC} = 240$  W in all the inductors. These power losses are computed by using manufacturer's dedicated software [15], where nonlinear characteristics of iron powder and dimensions of the core with a number of winding turns are taken into consideration.

The total power losses in the DC-DC converters  $P_{DCDCmax} = 630$  W are higher than power losses in the CHB converter and line inductors PCS ( $P_{PCSCmax} = 345$  W). The total efficiency of the PCS system operating at its worse conditions can be equal to approximately 90%. However, when the supercapacitors are charged and there is no need to deliver active power to the grid or to the sensitive loads, the DC-DC converters are turned off and the efficiency increases to 96.5%.

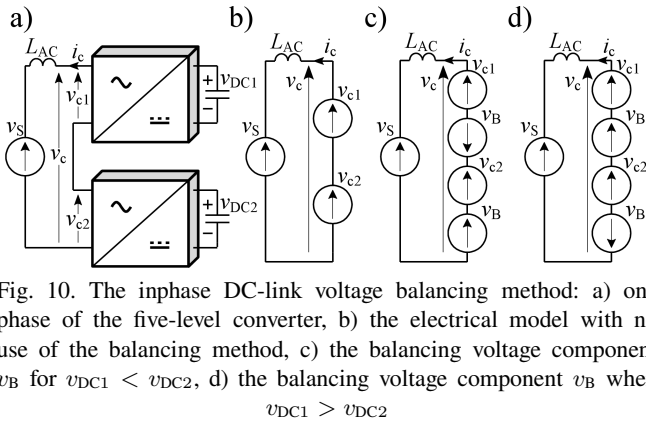
## 5. DC-link voltage balancing method

One of the most important problems that occur in multilevel converters is the problem of proper voltage balancing across DC-link capacitors. Because the proposed PCS is based on the cascaded converter, there are six separate DC-link capacitors the voltages of which have to be properly balanced [16, 17].

For controlling the DC-link voltages the voltage balancing method was developed [16]. This method is based on the interchange of energy between the converter cells (as presented in Fig. 2) that are connected in series in the same phase. Energy can be transferred between the cells only if the converter current  $i_c$  circulates continuously. The proposed method does not change the operation of the PCS and does not use the energy from the supercapacitor energy storage. For such a condition the cell with a higher DC-link voltage generates an additional output voltage component  $v_B$  that is in phase with the current  $i_c$  (delivers active power) The same component is subtracted from the output voltage ( $v_{c1}$  or  $v_{c2}$ ) of the cell with a lower DC-link voltage. Since the balancing voltage components have the same magnitudes and are out of phase, their sum is equal to zero, hence they do not change the output voltage  $v_c$ . The aforementioned procedure can be explained by means of a simple one-phase model of the voltage balancing method presented in Fig. 10 for three different cases. Because balancing is performed between the H-bridge converters inside a particular phase, this balancing method is called the inphase DC-link voltage balancing method.

The inphase DC-link voltage balancing method allows only the balancing energy to flow inside each of the phases separately and if the transfer of energy between the phases is needed, the interphase DC-link voltage balancing method can be applied. To fulfill the same assumption as in the first balancing method, the balancing component  $v_{B2}$  should be the zero sequence component of  $f_M$  frequency [8, 16].

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Unlike other voltage balancing methods used in CHB converters [18, 19], the proposed balancing method does not influence the AC side voltages generated by the converter ensuring the sinusoidal converter current  $i_c$ .

Both proposed DC-link voltage balancing methods have limitations when the modulating signals  $S_M$  exceed the carrier signals and the converter operates in the overmodulation region. The operation in close proximity to the overmodulation region can occur when the PCS generates large harmonic components. In the proposed DC-link voltage balancing method this drawback can be overcome by decreasing the amplitude of balancing components  $v_B$ , which increases the time of balancing. The test results of the operation of both DC-link voltage balancing methods are presented in Sec. 7.

### 6. Control of the power conditioning system

The control system of the PSC with a five-level CHB converter (Fig. 11) is divided into two separate parts; the first part is the controller of the CHB converter and the other one is the controller of six DC-DC converters. The controller of the CHB converter is similar to controllers of a power conditioning system with a two-level converter. The only difference between these controllers is the implementation of the DC-link voltage balancing method. The controllers of both CHB converters and DC-DC converters have a variable structure which is determined by fault signals generated in the mode detector – Fig. 12. Generally the controller of the CHB converter is responsible for controlling grid side currents of the PCS,  $i_c$ , or voltages across the sensitive load,  $v_{load}$ . The controller of the DC-DC converters is responsible for energy delivering to or taking from supercapacitors.

The mode detector (Fig. 12) generates three fault signals – a voltage dip fault signal  $F_U$ , overload fault signal  $F_I$  and supercapacitor discharge signal  $F_{DC}$ . The voltage dip signal  $F_U$  is active when the magnitude of the grid voltage space vector  $|V_S|$  decreases below 90% of its rated magnitude  $|V_{Sn}|$  and the time is longer than 2 ms. Signal  $F_U$  is reset when  $|V_S|$  increases above  $0.9 |V_{Sn}|$  and lasts for 20 ms. After 1 ms of overload the mode detector sets signal  $F_I$ . An overload is detected when d-axis component of the load current  $i_{loadd}$  exceeds the assumed maximum value  $i_{loaddmax}$ . To prevent oscillations between the overload and normal mode, a 1 ms

hysteresis is added to this signal. The signal  $F_{DC}$  is active when one of the fault signals  $F_U$  or  $F_I$  is set. Signal  $F_{DC}$  changes the controlled value in the DC-DC converter controller from supercapacitor voltages in the normal mode to DC-link voltages in the overload and voltage dip modes.

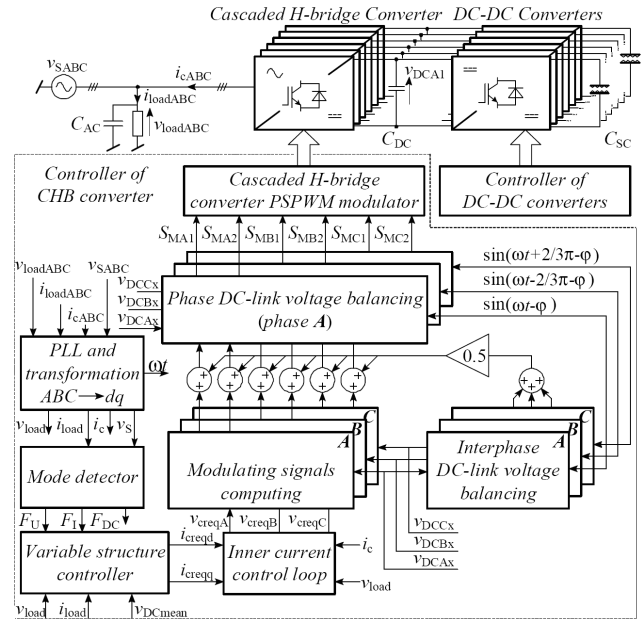


Fig. 11. A block diagram of the PCS controller

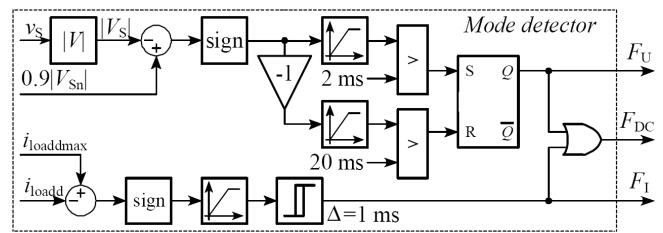


Fig. 12. A block diagram of the mode detector

Basing on fault signals, the variable structure controller controls different AC side variables (Fig. 13). In the normal mode the average value of all DC-link voltages  $v_{DCmean}$  is controlled. When the fault signal  $F_U$  is set, the load voltage is controlled and when the overload signal  $F_I$  is set, the CHB converter controller limits the line current d-axis component to its maximum value  $i_{loaddmax}$ . In the normal and overload mode the CHB converter generates additionally dq-axis components of the load current ( $i_{loadd}$  and  $i_{loaddq}$  respectively) to reduce reactive power and harmonics in the grid current. In the voltage dip mode both dq-axis components are determined by load voltage controllers REG2. To achieve satisfactory results, it is necessary to connect additional parallel capacitive filter  $C_{AC}$  to the sensitive load.

The inner current control loop generates CHB required converter voltage signals  $v_{creq}$  ensuring the required AC-side phase currents  $i_c$  with demanded dynamics similarly to [4].



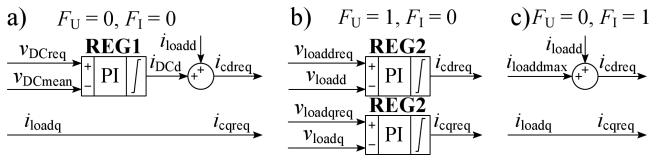


Fig. 13. Block diagram of the variable structure controller in the controller of CHB converter in: a) the normal mode, b) the voltage dip mode, c) the overload mode

The control system was implemented in the digital signal microcontroller TMS320F2808 and is described in more detail in [8].

## 7. Experimental results of the PCS

In this section a laboratory model of the power conditioning system based on a five-level cascaded converter with the supercapacitor energy storage (Fig. 14) and its experimental results have been presented.



Fig. 14. A laboratory model of the power conditioning system based on a five-level cascaded converter and supercapacitor energy storage (height 1 m, mass 300 kg)

The laboratory model of the PCS was designed and assembled according to the parameters presented in Table 1.

Table 1  
Parameters of the PCS laboratory model

Name of the parameter	Symbol	Value
rated power	$P$	10 kW
maximum supercapacitor energy	$E_{SC}$	313 kJ
line-to-line grid voltage	$V_{Sll}$	400 V
DC-link voltage	$V_{DC}$	190 V
rated supercapacitor voltage (1 from 6)	$V_{SCmax}$	120 V
AC-DC converter switching frequency	$f_N$	2.5 kHz
DC-DC converter switching frequency	$f_{NDC}$	15 kHz
line inductor inductance	$L_{AC}$	4 mH
DC-DC converter inductor inductance	$L_{DC}$	1 mH
DC-link capacitor capacitance	$C_{DC}$	4 mF
supercapacitor capacitance (1 from 6)	$C_{SC}$	7.25 F
short-circuit power of the grid	$S_n$	1 MVA

**Start-up of the PCS**. Starting the PCS after its disconnection from the grid is the procedure that is called the start-up. During this procedure the DC-link capacitors and supercapacitors are charged from the grid. First, the DC-link capacitors have to be charged to the rated voltages  $V_{DC}$  and then the charging process of the supercapacitors starts. For ensuring the proper shape of the grid currents, the DC-link voltages should be high enough. Safe charging can be performed by connecting the inrush resistors  $R_i$  between the grid and the PCS. This procedure is well known from classical two-level converters operating as front-end converters e.g. in adjustable speed drives. However, in a two-level converter there is one DC-link voltage and because of the cost there can be only one inrush resistor in the DC-link circuit. In the case of a five-level cascaded converter, due to six separate DC-link circuits, a better solution is to use three inrush resistors at the grid side, as presented in Fig. 15.

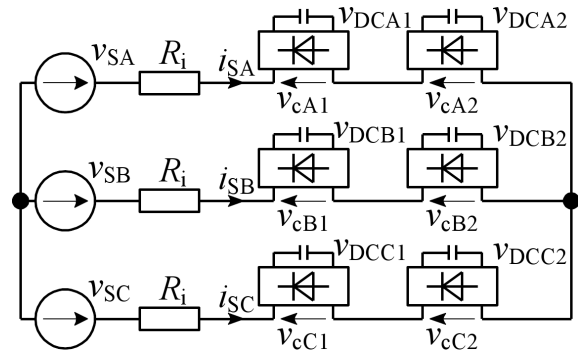


Fig. 15. A model of the PCS for the beginning of the start-up (line inductors  $L_{AC}$  and line impedance are neglected)

The DC-link voltages during the start-up rise to the value of  $V_{DC1} = \sqrt{2}V_{Sll}/4 = 141$  V, for  $V_{Sll} = 400$  V. To explain the reason why  $v_{DC} = V_{DC1}$ , one can use the model circuit shown in Fig. 15.

As long as the capacitors are charged, the CHB converter diodes conduct. The DC-link capacitors are charged to the voltage at which the currents  $i_{SA}$ ,  $i_{SB}$  and  $i_{SC}$  flow for a very short time. These currents only flow in the loop between two phases where the line-to-line grid voltage operates as a source and the output voltages  $v_{cA1}-v_{cC2}$  have such signs that yield to Kirchhoff's voltage law. As voltages  $v_{DCA1}-v_{DCC2}$  always have positive values of  $v_{cA1}-v_{cC2}$  and assuming that each DC-link voltage is the same and equal to  $V_{DC1}$ , the Kirchhoff's voltage law can be written as (14).

$$\sqrt{2}V_{Sll} = 4V_{DC1}. \quad (14)$$

When the DC-link voltages reach  $V_{DC1}$ , the PCS transistors start to operate in the manner to deliver energy into the DC-link capacitors maintaining the grid currents  $i_S$  sinusoidal. The whole start-up process with the waveforms of one of the six DC-link voltages, grid current  $i_S$  and grid phase voltage  $v_S$  has been presented in Fig. 16.



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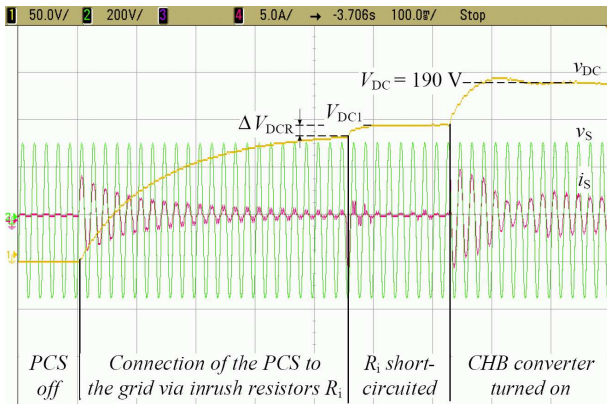


Fig. 16. The start-up of the laboratory model of the PCS

From Fig. 16 it can be seen that the inrush resistors  $R_i$  are short-circuited when the DC-link voltage is close to  $V_{DC1}$ . If the difference voltage  $\Delta V_{DCR}$  is smaller, the start-up process will last longer and the greater the voltage  $\Delta V_{DCR}$ , the greater the inrush current  $i_S$  is. After the voltage  $v_{DC}$  reaches  $V_{DC1}$ , the converter is switched on and the DC-link voltage increases to  $V_{DC} = 190$  V.

**PCS operation during a voltage dip.** If the rms value of the grid voltage decreases below 90% of its rated value and lasts more than 2 ms, a voltage dip is detected. In this case the PCS turns off the grid switch (presented in Fig. 1) and tries to restore the load voltage to its rated value. During this operation the PCS delivers energy to the load at a cost of supercapacitor energy. For longer voltage dips, which cause a greater consumption of energy than energy stored in supercapacitors, it is necessary to use higher energy sources e.g. diesel motors. When the voltage dip finishes, the PCS starts operating in its normal mode (reactive power compensation and harmonic elimination) and also delivers energy back to the supercapacitor storage.

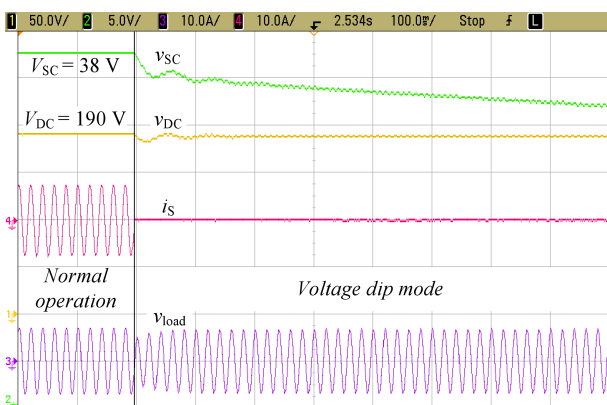


Fig. 17. The PCS operation during a grid voltage dip; time scale: 100 ms/div

The waveforms showing the reaction of the PCS to a voltage dip are presented in Fig. 17. In this figure the voltage dip is modelled by the interruption in three phases at the same time ( $i_S = 0$ ) and at this moment the energy is taken from

supercapacitors ( $v_{SC}$  decreases) keeping the same load voltage. The figure shows that the amplitude of the voltage  $v_{load}$  slightly differs. It is caused by the fact that the PCS produces voltages without harmonics which are present in the grid voltage and the amplitude of this voltage is equal to its nominal value.

**Operation of the DC-link voltage balancing method.** Figure 18 presents two DC-link voltages in phase A,  $v_{DCA1}$  and  $v_{DCA2}$  of the PCS when the inphase DC-link voltage balancing voltage method is applied. It can be seen that there is no influence of this method on the phase current  $i_{cA}$ , which proves the correctness of the proposed balancing method.

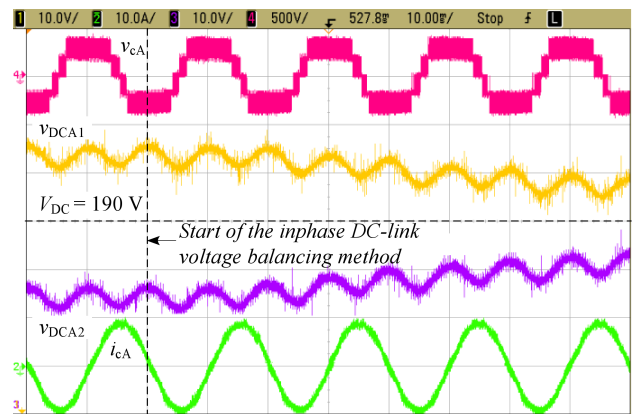


Fig. 18. The operation of the inphase DC-link voltage balancing method applied in the laboratory model of the PCS

The application of both DC-link voltage balancing methods allows proper balancing of all DC-link voltages. In Fig. 19 one can see that the balancing process lasts  $t_B = 330$  ms. This time depends on the amplitude of the balancing voltage components  $v_B$  and  $v_{B2}$  and the amplitude of the PCS current  $I_{cm}$ . Higher amplitudes result in shorter balancing times  $t_B$  but at the cost of higher distortion of the modulating signals  $S_M$  and higher possibility of overmodulation.

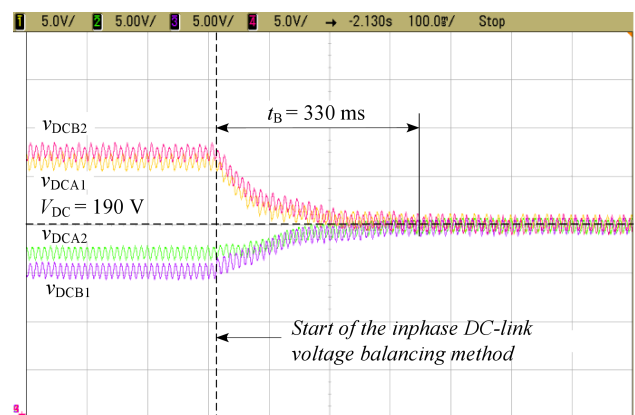


Fig. 19. The inphase and interphase DC-link voltage balancing methods operation in the laboratory model of the PCS

## 8. Conclusions

The presented power conditioning system based on a five-level cascaded H-bridge converter with supercapacitor energy storage can improve power quality from the point of view of both the grid and sensitive loads. Taking into account all the operating conditions, it can be noted that the PCS always operates with a slightly changeable amplitude modulation index. The paper contains a thorough power losses analysis, which can be useful for designing of the PCS. The calculated power losses obtained in the analysis presented in this paper have given results which have been correctly verified in a laboratory test for reactive power compensation up to  $Q_{\text{load}} = 10$  kVA.

The proposed DC-link voltage balancing method based on additional balancing voltage components was successfully verified by experimental tests and it can be used in multilevel cascaded converters with different voltage levels.

The assembled laboratory model of the PCS operates properly under all assumed conditions, which was proved by experimental test results. As it was described, the PCS can increase power quality in a different manner depending on the conditions of the grid or the sensitive loads.

Multilevel converters offer good and very flexible solutions for different medium voltage applications. The proposed five-level cascaded H-bridge converter operating in the PCS was connected to the low voltage distribution grid ( $V_{\text{SN}} = 400$  V), but its topology allows it to be used with medium voltages up to 6 kV. It also seems that the CHB converter, due to its modularity, is the best converter for the power conditioning system with supercapacitor energy storage.

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